Integrated Circuit 2: Examination

※ メモなし講義資料(手書きの書き込みも可)・自筆ノート・書籍のみ持込可。

※ 解答は導出過程を含めてすべて答案用紙(日本語でも英語でもよい)に記入すること。

1. Let's discuss on the architecture of adders. Assume the i-th bit of input signals A and B to be Ai and Bi, respectively, and the i-th bit of the sum and the carry output to be Si and Ci, respectively. Assume that the generation and the propagation term in i-th bit to be Gi and Qi, respectively. (25)

(1) Write Gi and Qi in Boolean expression.

(2) The propagation term, Qi, can be described using logical-OR, instead of exclusive-OR. Answer the reason why.

(3) Write Si and Ci in Boolean expression using Gi and Qi.

(4) Write C0, C1, C2, and C3 with using the carry look-ahead architecture in Boolean expression of Ai and Bi.

2. Figure 1 illustrates the operation waveform of DRAM cell array for 4 bits, whose circuit configuration is shown in Fig.2. Answer the status (charged or discharged) of each capacitor in initial condition for C1 to C4; write '1' for charged, and '0' for discharged. Answer the reason briefly why you have chosen their status. Note that PRE and SA are the pre-charge and the sense amplifier control signal, respectively, and the circuits for pre-charge and sense amplifier are not shown in Fig.2, but assume that these circuits are correctly connected. (25)



3. Discuss the characteristics of the capacitor-array D/A converter implemented on LSI, in terms of the accuracy and the circuit (area) size. The terms of "rational accuracy" (「比精度」in Japanese) MUST be included. (20)

4. 【予告問題】Discuss the topic on "MOSFET's Scaling, or Moore's Law" in terms of social, technical, and economical impacts. Your opinion AND your personal experience MUST be included. Write it down on A4-size paper (hand-written material only, in Japanese or English). (20)

5. Describe your reflection (振り返り) and impressions on what you have learnt in this class, in terms of how they effect your daily and long term life, and the context you have learnt in other classes. (10)