Integrated Circuit 2B Examination / Integrated Circuit2 Term Examination

2020/2/3(Mon)　08:45～10:15@102

※ メモなし講義資料(手書きの書き込みも可)・自筆ノート・書籍のみ持込可。
※ 解答は導出過程を含めてすべて答案用紙(日本語でも英語でもよい)に記入すること。
※ 動作波形の表示では、変化のタイミングが一致する箇所を縦点線にあわせ、必要に応じて縦点線を追加すること。

1. Figure 1 shows the configuration of 2x2bit DRAM circuit. Here, The "Sense Amp & Precharge" block is the circuit composed of the sense amplifier and precharge control, and "PRE" and "EN" are the precharge control signal and the sense amplifier enable signal, respectively. The memory cell capacitors are either discharged("0") or charged("1") at initial. Draw the waveform of DL0, DL0b, DL1 and DL1b for the control signal in Fig.A (in answer sheet). Note that V_{DP}, $V_O^{(1)}$, and $V_O^{(0)}$ are the voltages of the precharged state, DL voltage for "1" readout, and DL voltage for "0" readout, respectively.(60)

2. Figure 2 shows the configuration of 2bit mask ROM. Draw the waveform of D for the control signal in Fig.B (in answer sheet). Note that D is precharged to V_{DD} when PRE=1. (15)

3. Figure 3 shows the configuration of 4bit Flash A/D converter. Draw the waveform of Q0, Q1, Q2 and Q3 for the input waveform of Vi in Fig.C (in answer sheet). Note that the output of the comparator becomes "1" when the voltage of "+" input is higher than that of "−".(10)

4. Describe your reflection（振り返り） and impressions on what you have learnt in this class, in terms of how they effect your daily and long term life, and the context you have learnt in other classes. (10)

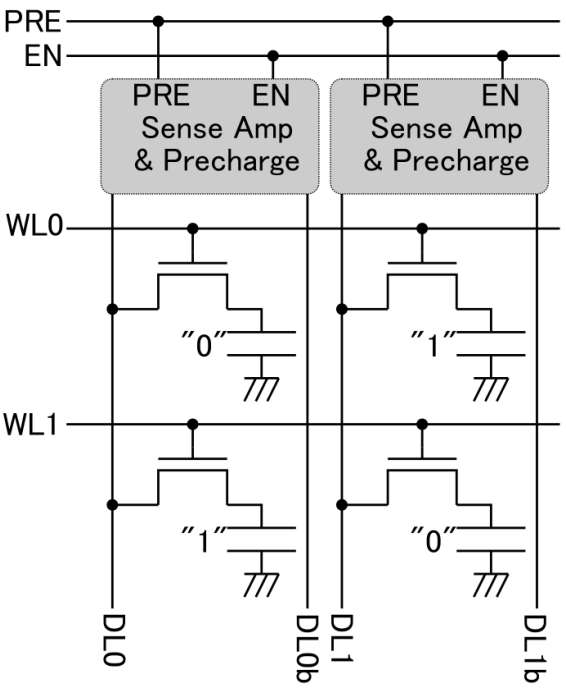


Fig.1

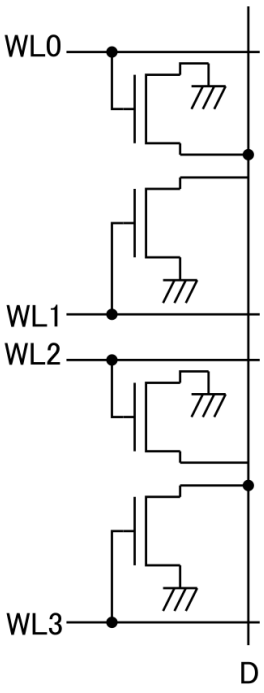


Fig.2

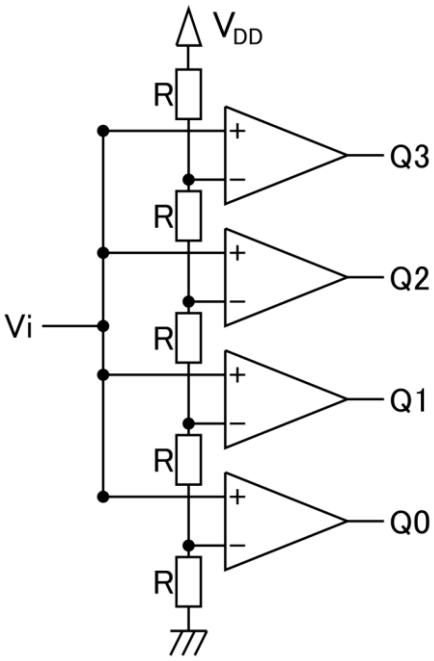
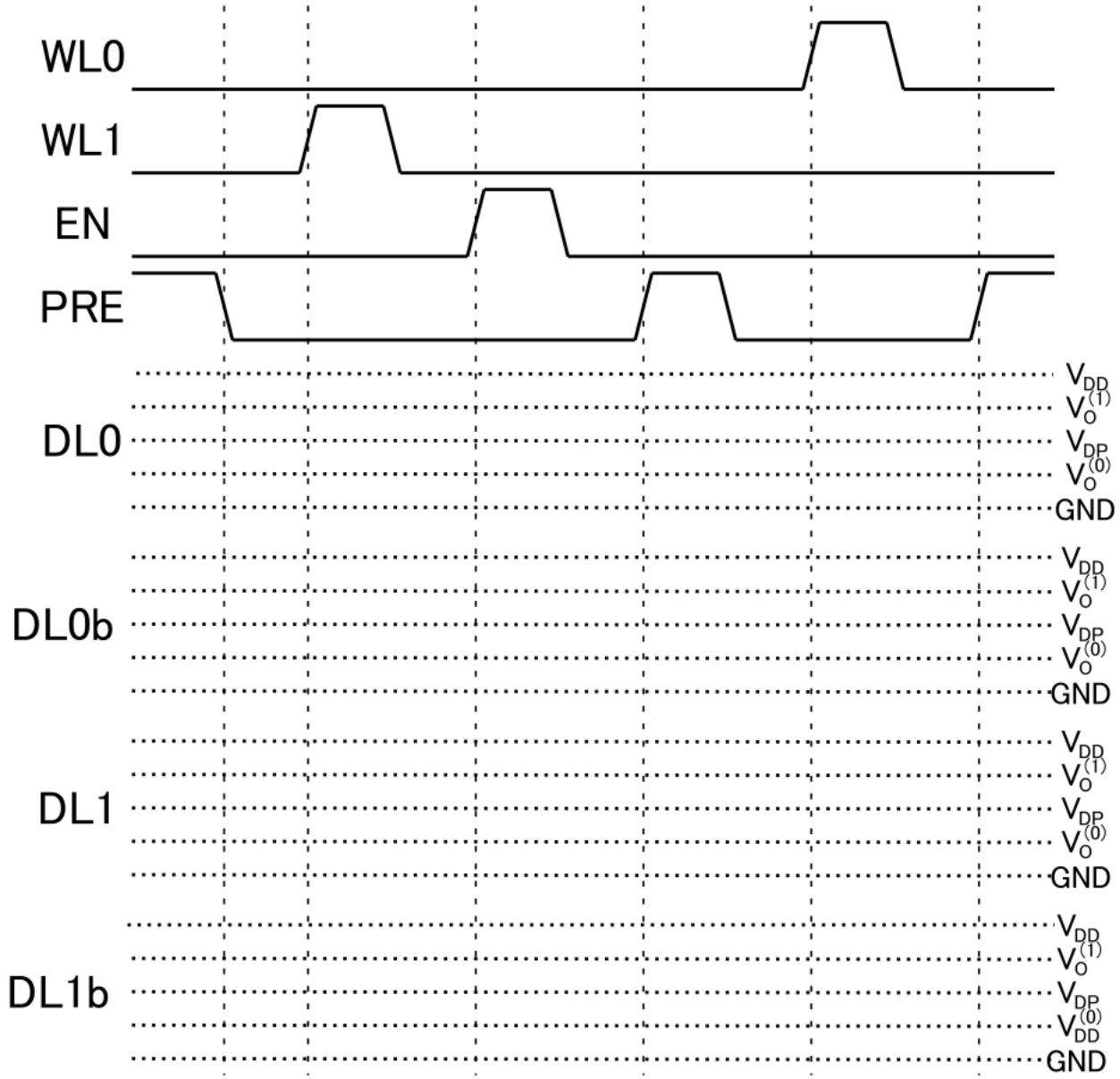


Fig.3

Integrated Circuit 2B Examination / Integrated Circuit2 Term Examination Answer Sheet

名列番号 名前

1.



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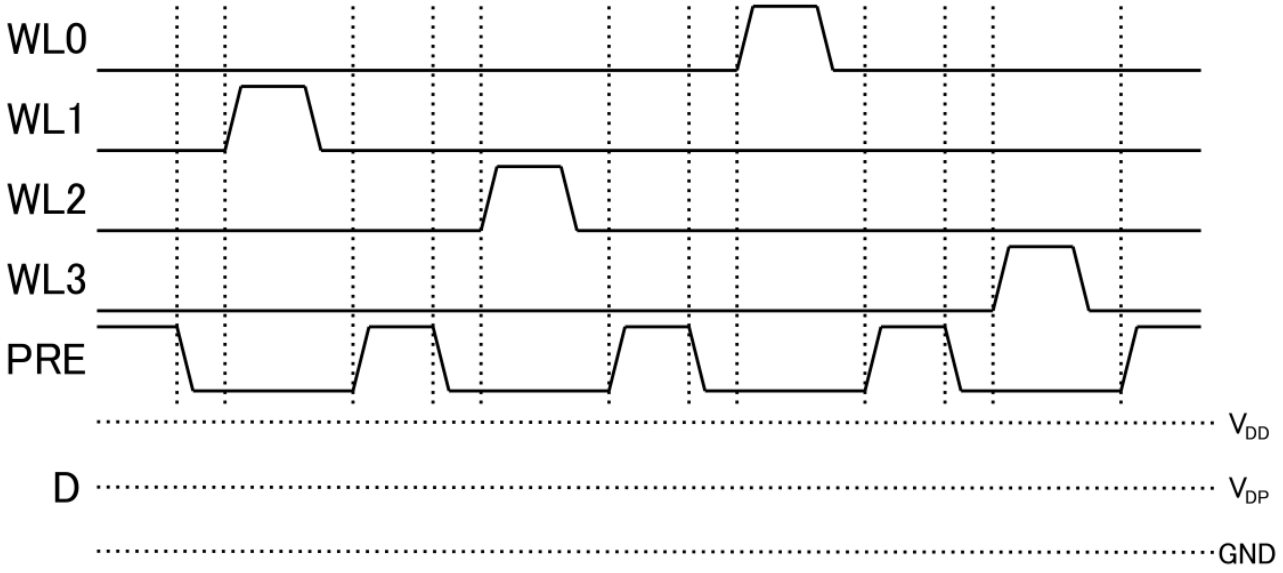

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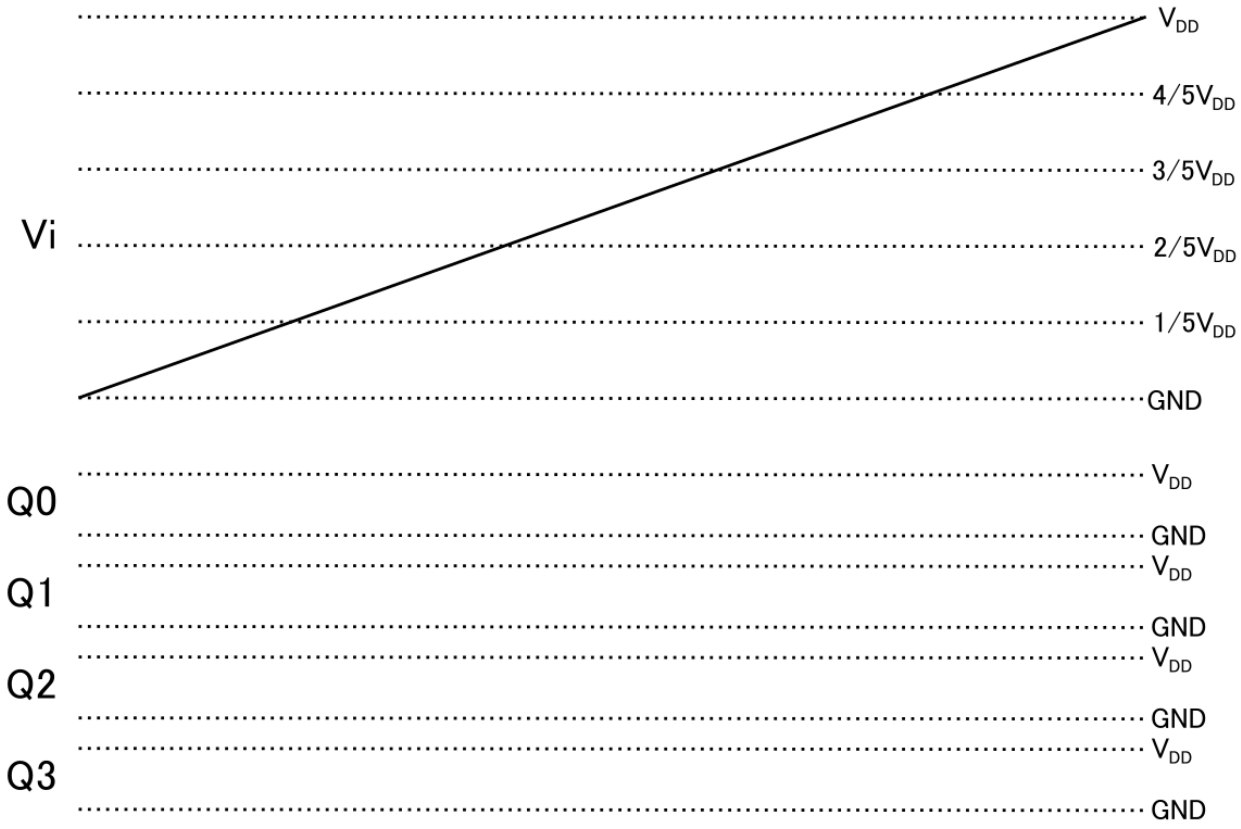
V_{DD}
$4/5V_{DD}$
$3/5V_{DD}$
Vi
$2/5V_{DD}$
$1/5V_{DD}$
GND
V_{DD}
Q0
GND
V_{DD}
Q1
GND
V_{DD}
Q2
GND
V_{DD}
Q3
GND

4.