Integrated Circuit D Final Report

※結果だけでなく、導出過程を含めて記述すること。また講義資料以外で参考にしたものがある場合(Web ページや友人との相談も含む)は、必ず出典を明記すること。出典を示さずに引用が確認された場合は不正行為とみなします。また解答は日本語でも英語でもよい。

出典の表記形式(例)

・秋田純一「はじめての電子回路 15 講」, p.10-12 （※書籍の場合。著者名、書名、ページ）:

・http://ifdl.jp/akita/class/ （※Web ページの場合。URL）

・○○君と相談 （※友人等との相談の場合）

1. Figure 1 shows the configuration of 8bit NAND-type mask ROM circuit, where each block has 4 bits. Assume that the read access for blocks are performed followed by the precharge for D. MOSFETs with "*" indicated has the negative threshold voltage (Vt<0), while others have positive threshold voltage (Vt>0). Answer the value of D (0 or 1) and the ON/OFF state (○/×) of MOSFETs M0–M9 for the inputs in Table 1.(60)

2. Figure 2 shows the configuration of 4bit Flash A/D converter. Draw the waveform of Q0, Q1, Q2 and Q3 for the input Vi that linearly changes from (t, v)=(0s, 0V) to (10ms, V_{DD}). Indicate the timing of Q0–Q3 change clearly with the corresponding voltage. Note that the output of the comparator becomes "1" when the voltage of "+" input is higher than that of "–".(20)

3. Assume that you are planning to start a new business. Discuss the possible small-lot LSI application in your business, as well as your business plan. For example, IoT health monitoring, IoT smart agriculture, and so on. (10)

4. Describe your reflection （振り返り） and impressions on what you have learnt in this class, in terms of how they effect your daily and long term life, and the context you have learnt in other classes. (10)
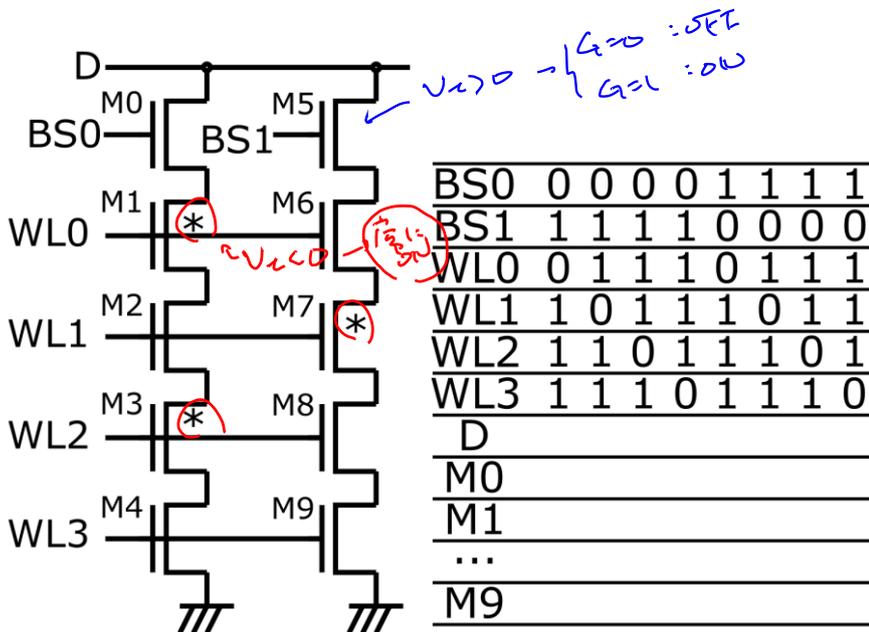

Fig.1

BSO	0	0	0	0	1	1	1	1
BS1	1	1	1	1	0	0	0	0
WL0	0	1	1	1	0	1	1	1
WL1	1	0	1	1	1	0	1	1
WL2	1	1	0	1	1	1	0	1
WL3	1	1	1	0	1	1	1	0
D								
M0								
M1								
...								
M9								

Table 1
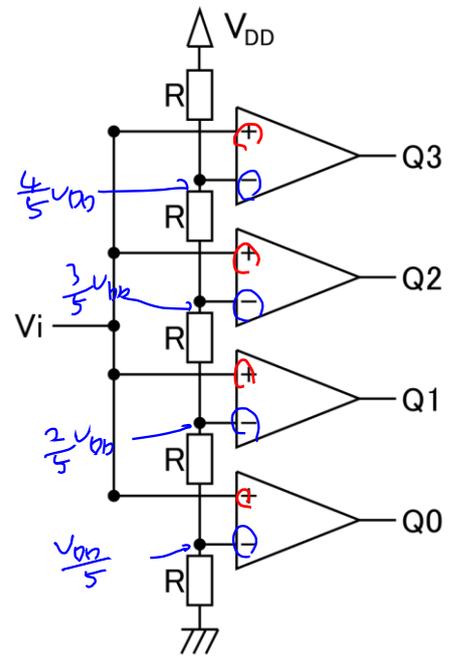
Fig.2

1

BS0	0	0	0	0	**1**	**1**	**1**	**1**
BS1	**1**	**1**	**1**	**1**	0	0	0	0
WL0	(0)	1	1	1	(0)	1	1	1
WL1	0̶	(0)	1	1	1	(0)	1	1
WL2	1	1	(0)	1	1	1	(0)	1
WL3	1	1	1	(0)	1	1	1	(0)
D	1	(0)	1	1	(0)	1	(0)	1

右側注記（緑）:
{ BS1=1, WL1=1 } "0を記憶している"
{ BS0=1, WL0=1 }   に (*)をおく
{ BS0=1, WL2=1 }

BS0 → M0	X	X	X	X	(0)	0	(0)	0	
M1	0	0	0	0	0	0	0	0	← (*)
M2	0	X	0	0	0	X	0	0	← WL0+1
M3	0	0	0	0	0	0	0	0	← (*)
M4	0	0	0	X	0	0	0	X	← WL3
BS1 / BS2 → M5	0	0	0	0	X	X	X	X	
M6	X	0	0	0	X	0	0	0	← WL0
M7	0	0	0	0	0	0	0	0	← (*)
M8	0	0	X	0	0	0	X	0	← WL2
M9	0	0	0	X	0	0	0	X	← WL3

放電

2.

V_{DD}

$\frac{4}{5} V_{DD}$

$\frac{3}{5} V_{DD}$

$\frac{2}{5} V_{DD}$

$\frac{1}{5} V_{DD}$

"1"

V_i

Q_0 Q_1 Q_2 Q_3

O

t

10 ns