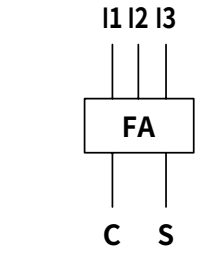
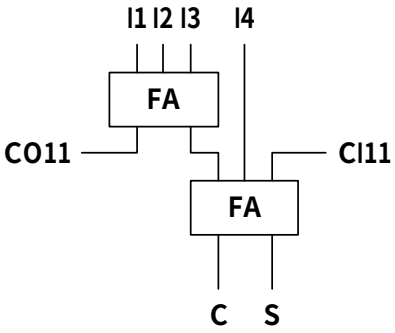
集積回路工学第２　第９回資料

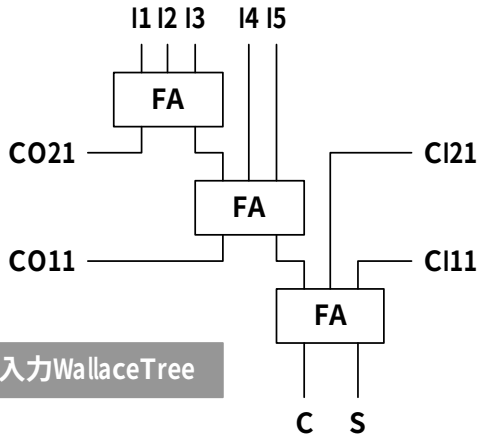
ワレスの木(Wallace Tree)



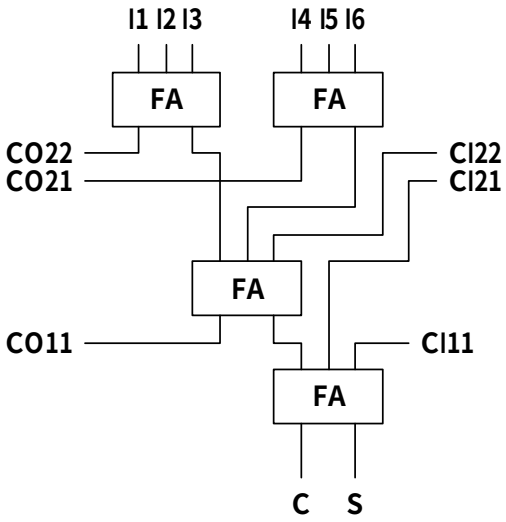
3入力WallaceTree



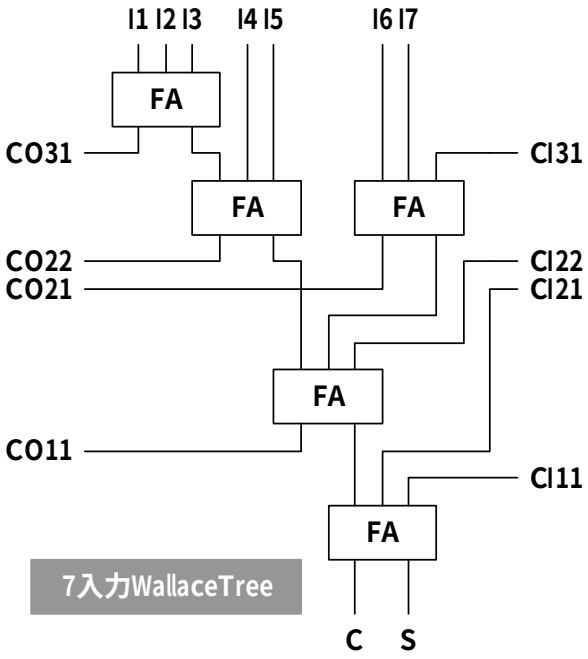
4入力WallaceTree



5入力WallaceTree



6入力WallaceTree



7入力WallaceTree

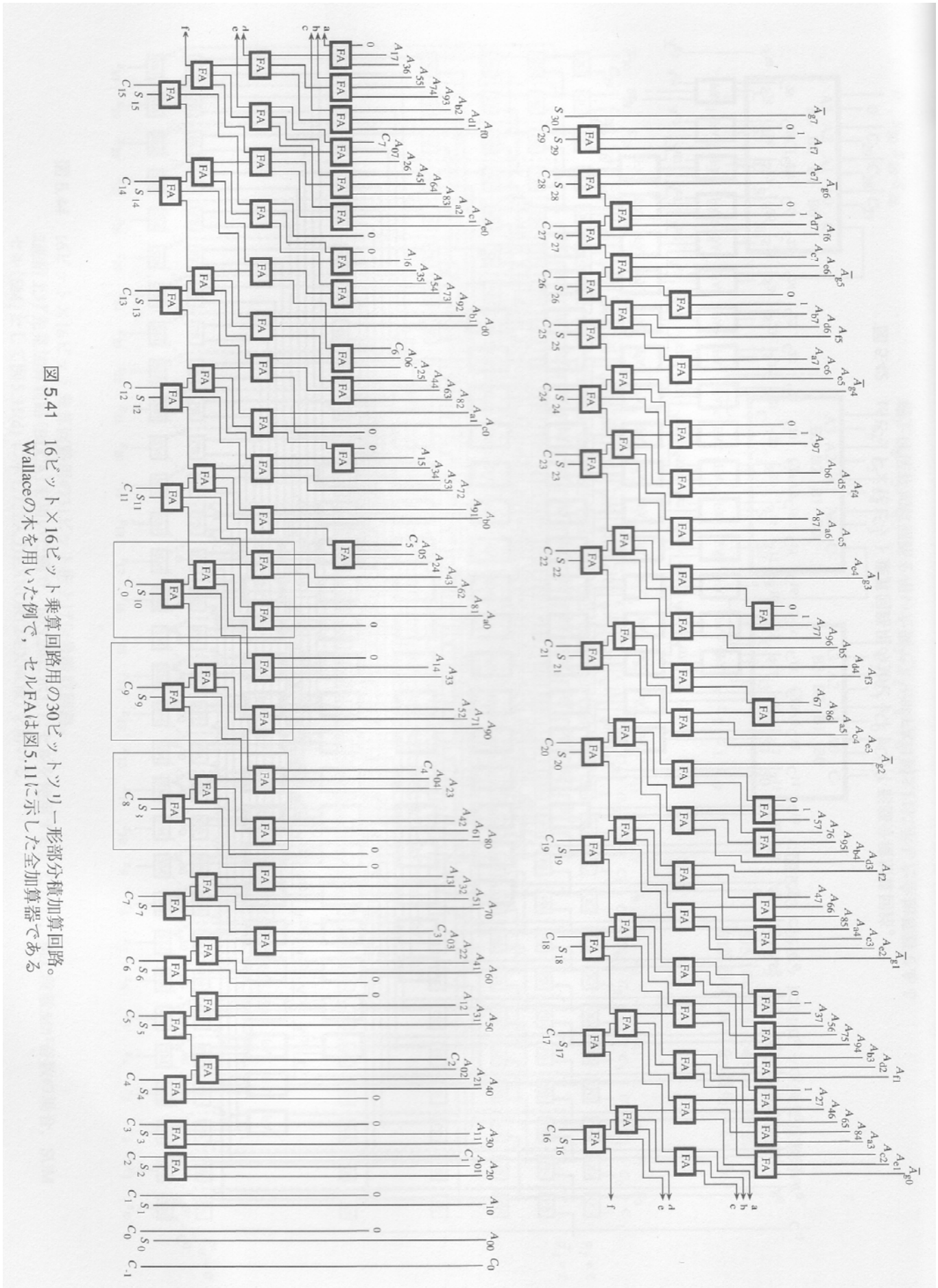


図 5.41　16ビット×16ビット乗算回路用の30ビットツリー形部分積加算回路。Wallaceの木を用いた例で，セルFAは図5.11に示した全加算器である

(出典: 榎本忠義「CMOS 集積回路」p.169 より抜粋)