

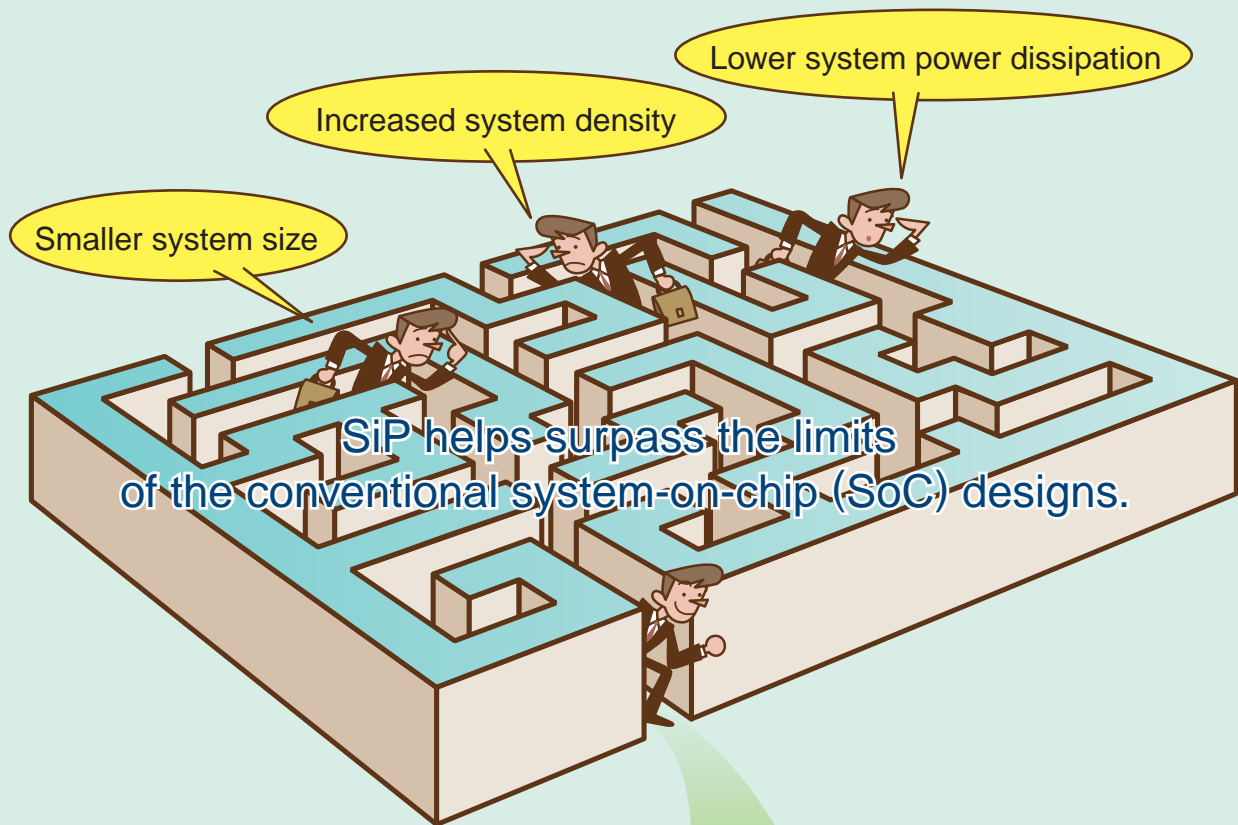
TOSHIBA

SYSTEM CATALOG

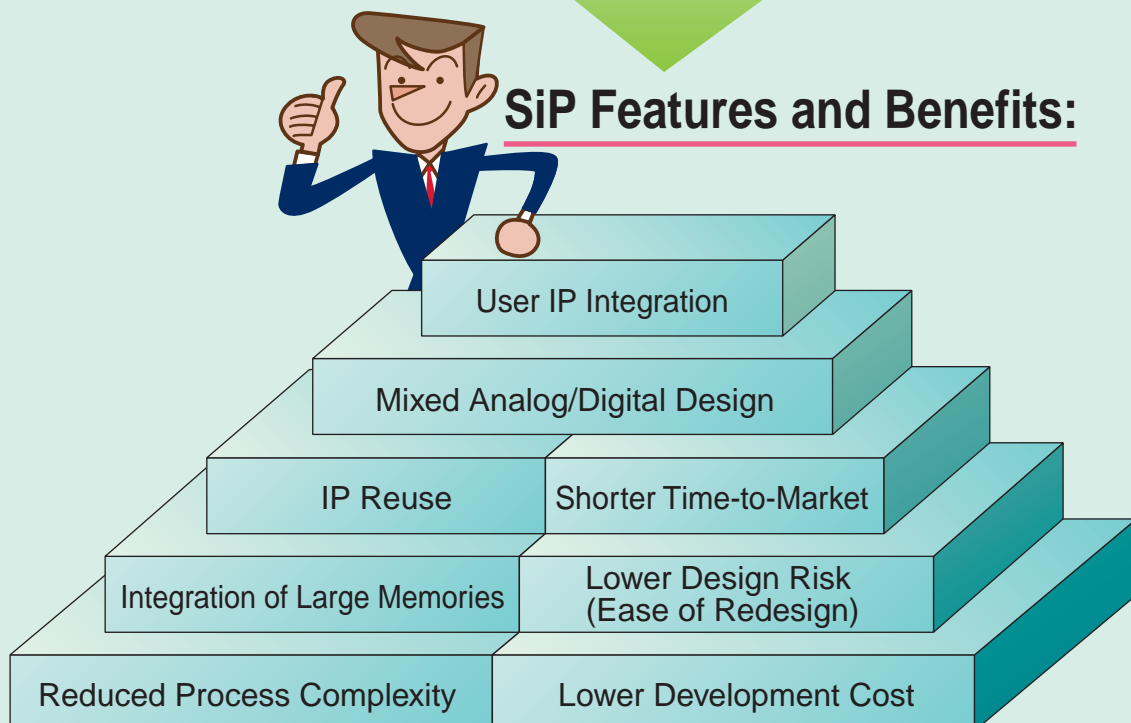
SiP (System in Package)

2004 semiconductor
<http://www.semicon.toshiba.co.jp/eng>

SiP provides a solution to system design challenges.

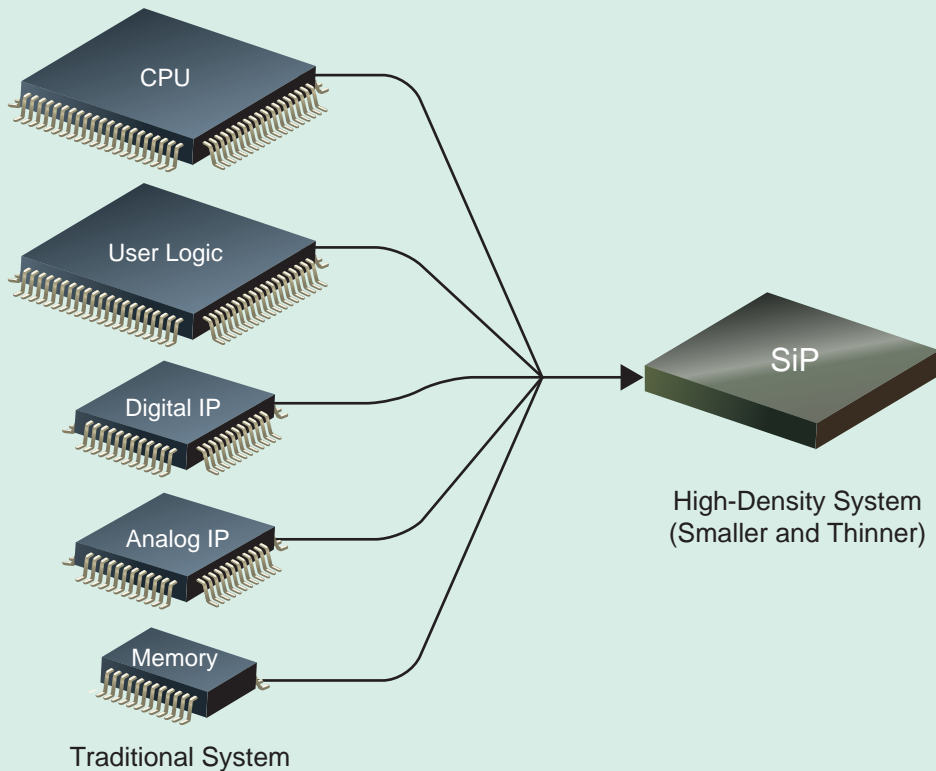


SiP Features and Benefits:



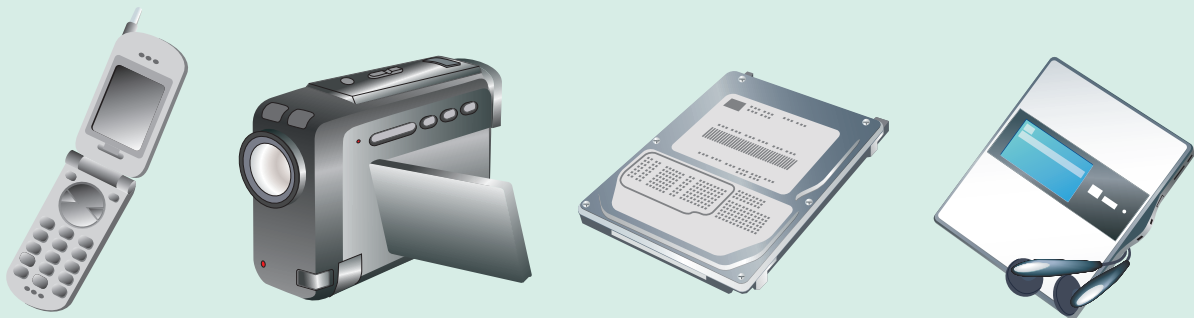
What is System-in-Package (SiP)?

SiP is an advanced technology to incorporate multiple components into a single package. You can mix a variety of components such as CPU, logic, analog and memory functions, reducing overall system size.



Market Needs for SiP

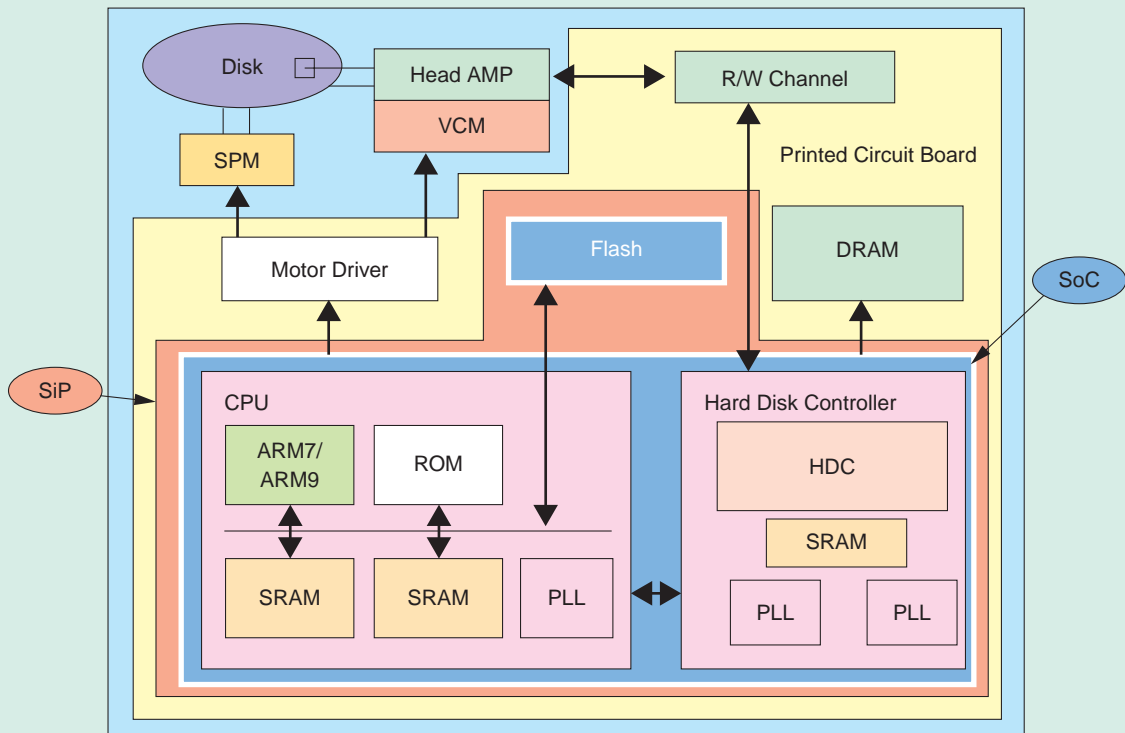
1. Reducing system board space
 2. Reducing board mounted height
- The evolution of mobile electronic devices such as cell phones, digital cameras, digital camcorders and portable audio players is driving the demand for SiP solutions.



System Block Diagram Examples

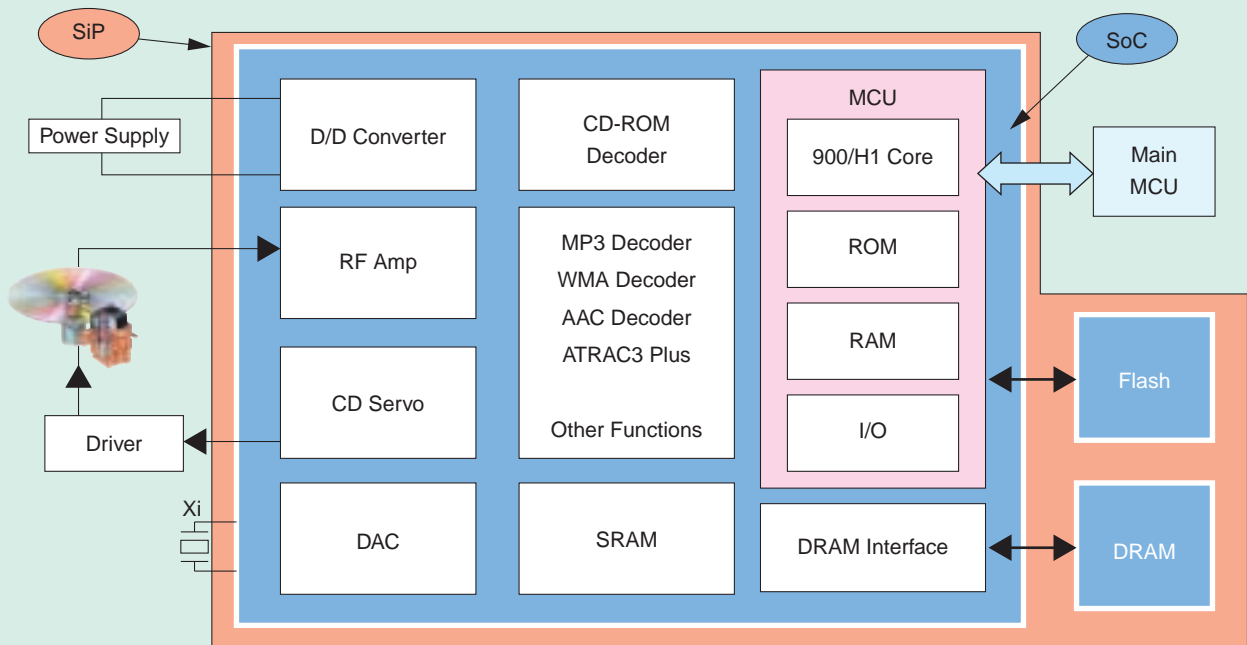
1. Ultra-Thin Hard Disk Drive

2-Chip SiP (SoC + Flash)



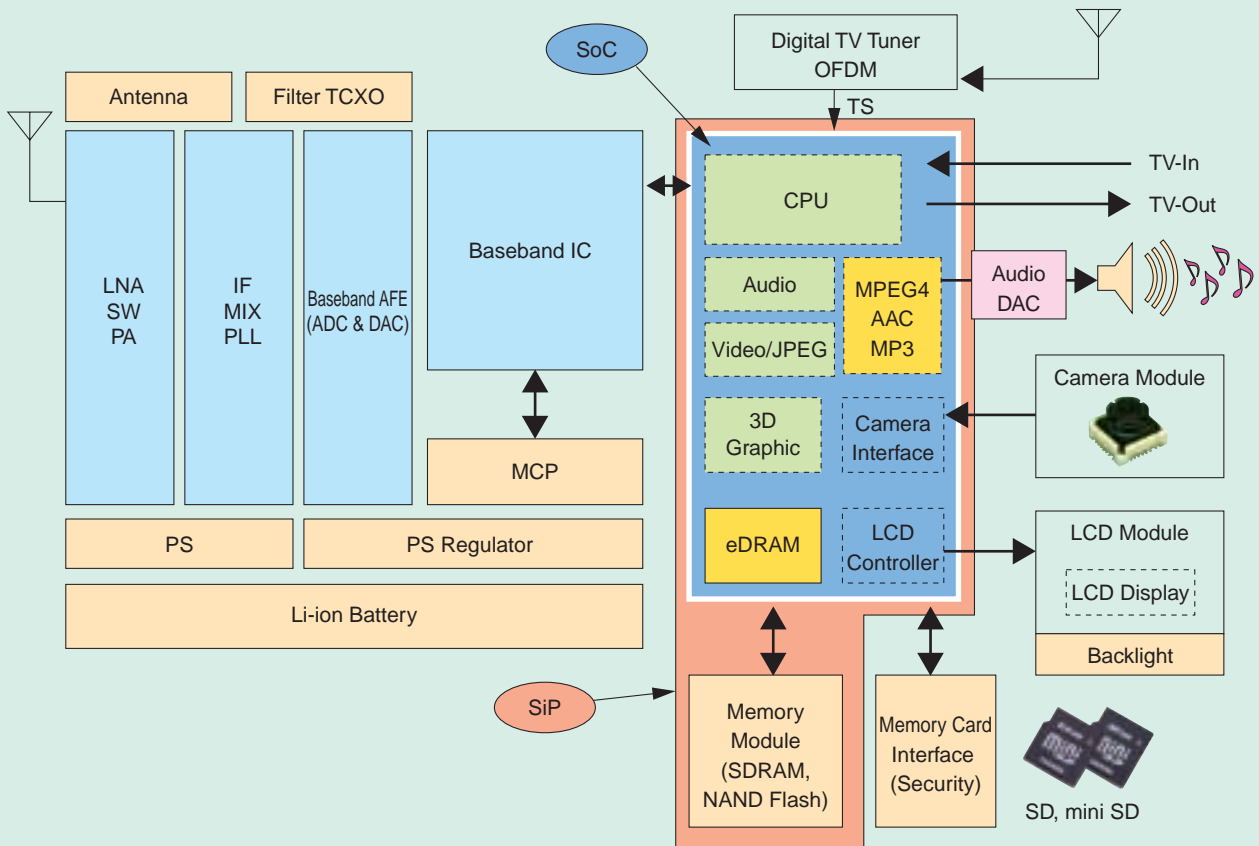
2. CD/MP3 Player

3-Chip SiP (SoC + Flash + DRAM)



3. Cell Phone

3-Chip SiP (SoC + SDRAM + NAND Flash)



MP3: MPEG Audio Layer 3. Audio compression standard developed by the Motion Picture Experts Group (MPEG), a working group in the International Standards Organization (ISO).
 WMA: Windows Media Audio. Proprietary compressed audio file format used by Microsoft Corp. Features a high compression ratio and high-quality sound close to CD.
 ACC: MPEG-2/Advanced Audio Coding. International audio compression standard developed by the MPEG group.
 ATRAC3 Plus: Adaptive TRansform Acoustic Coding 3 Plus. Audio compression algorithm developed by Sony Corp.

CPU

- TX99
- TX49
- TX39
- TX19
- TLCS-900/H1
- TLCS-900/L1
- ARM7
- ARM9
- MeP

Memory (Incl. Third-Party Products)

- NOR Flash
- NAND Flash
- FCRAM
- SDRAM/DDR-SDRAM

User Logic

- 0.18 μm
- 0.13 μm
- 90 nm

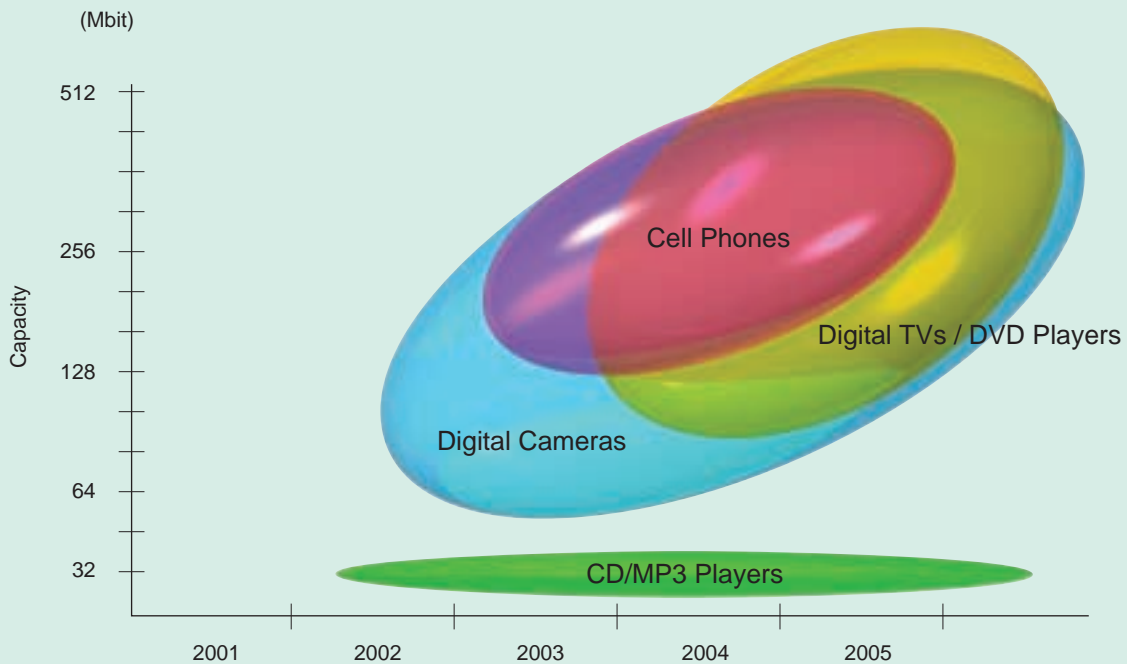
Digital IP

- USB 2.0
- IEEE1394
- 10/100BASE Ethernet MAC
- Audio Codec (MP3, etc.)

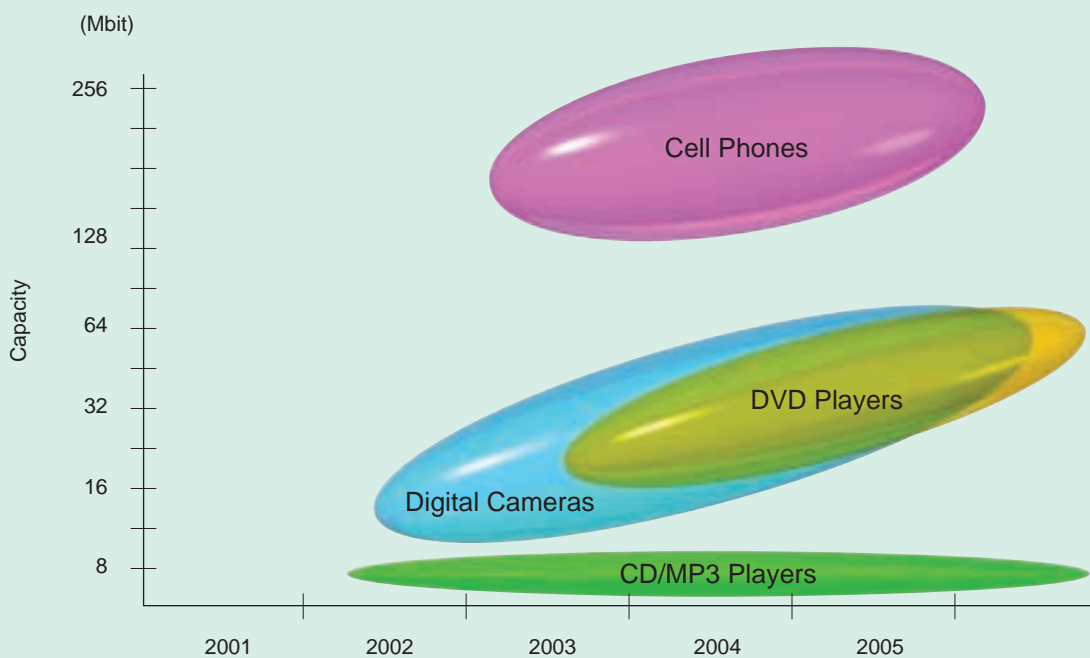
Analog IP

- DC-DC Converters
- A-D Converters
- A-D Converters

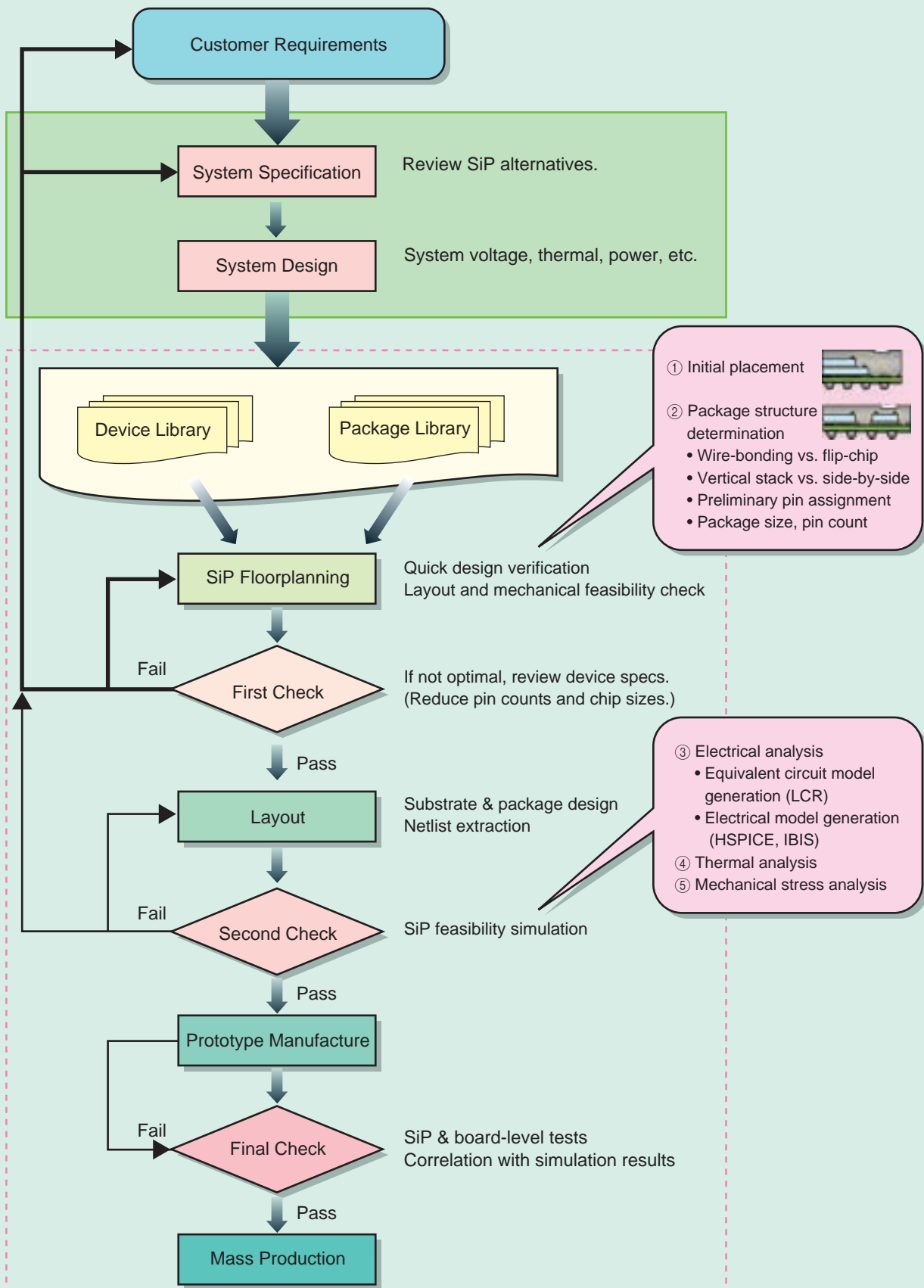
SDRAM



Flash

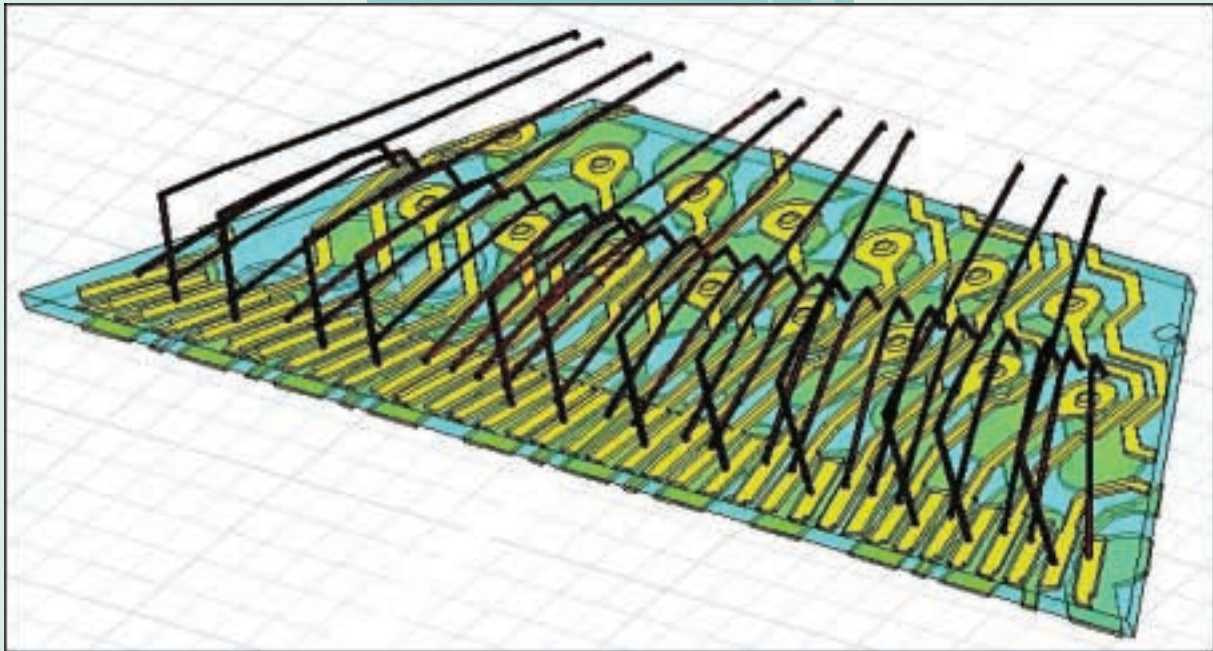


SiP Development Flow



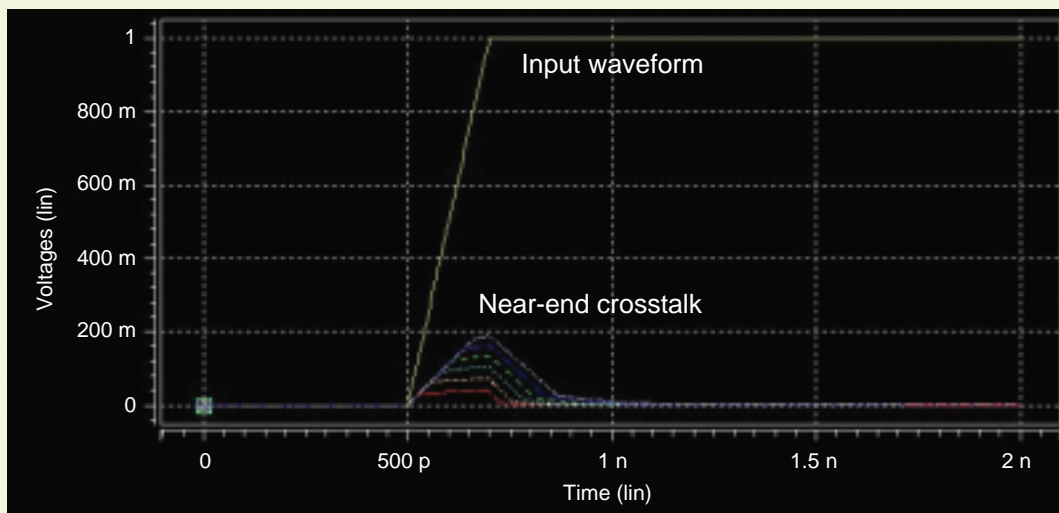
If you are concerned about electrical noise,

Toshiba offers 3-D electrical modeling services.



3D Electrical Model Example

Near-End Crosstalk Noise

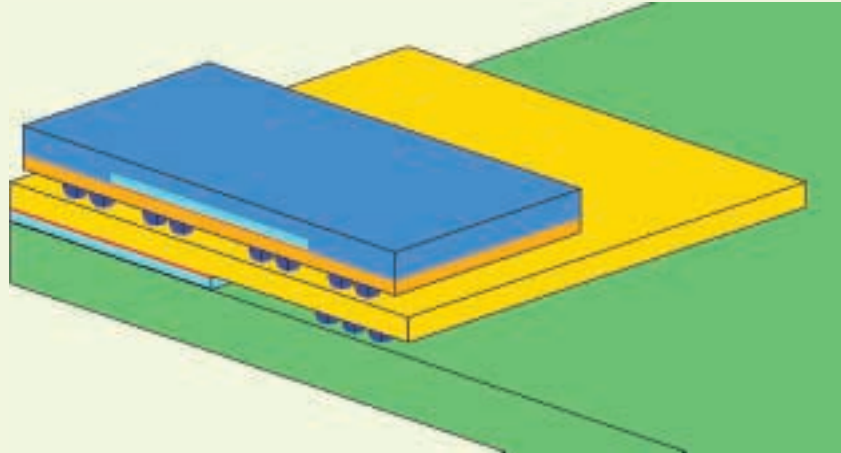


Tr (Edge Rate) = 200 ps

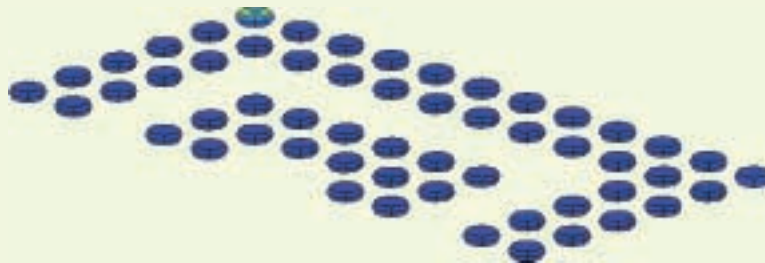
To assist you with analysis of signal integrity problems such as crosstalk, Toshiba offers RLC extraction and HSPICE/IBIS modeling for electrical simulation.

If you are concerned about the solder interconnect reliability,

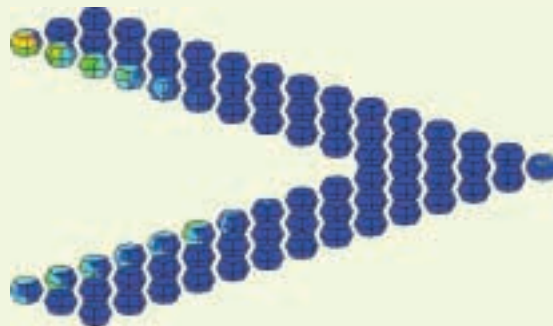
Toshiba offers 3-D solder stress analysis services.



SiP Stress Analysis Model



Solder Bump Strains in the Upper BGA

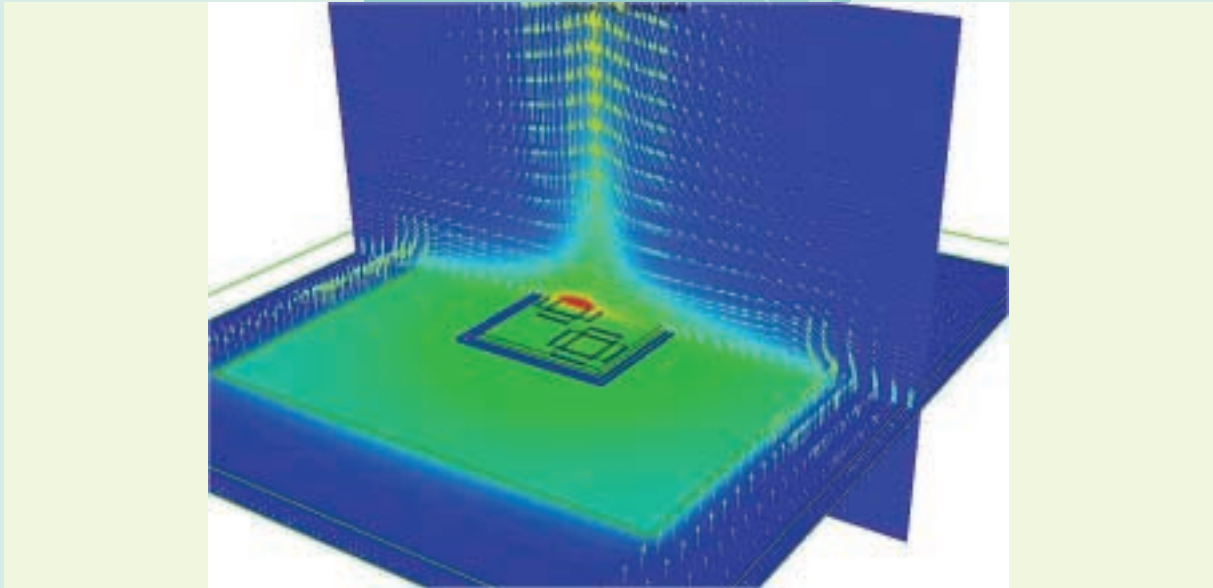


Solder Ball Strains in the Lower BGA

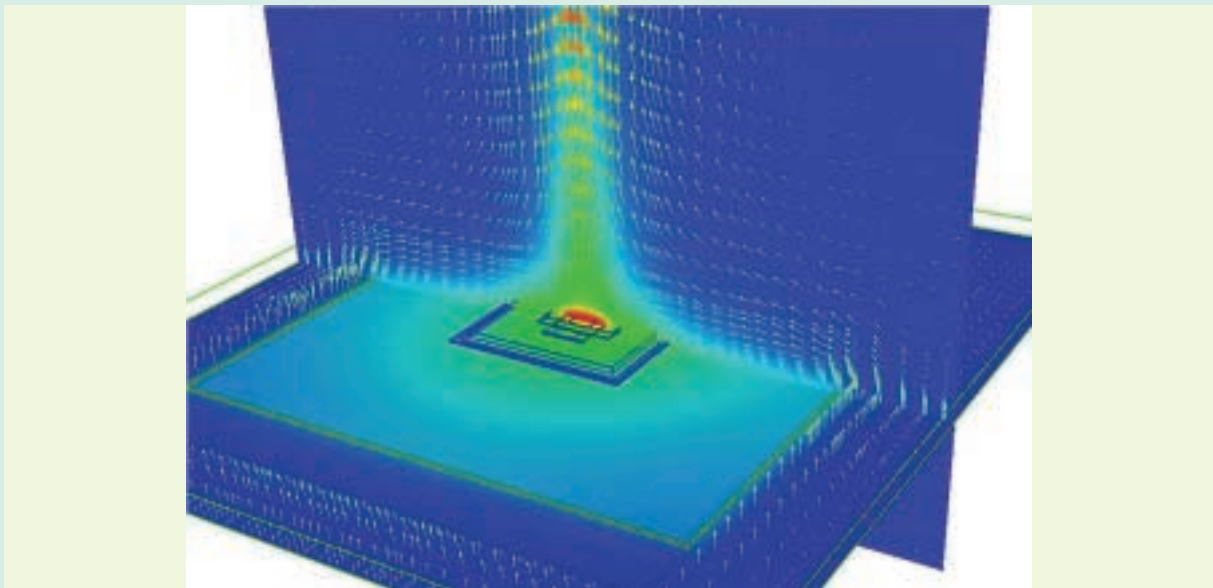
Toshiba provides support for measuring stress-induced strains in solder joints. Thermo-mechanical deformations of solder joints can be used for lifetime prediction, with the objective of studying solder joint reliability.

If you are concerned about thermal issues,

Toshiba offers 3-D thermal analysis services.



Thermal Flow for a Side-by-Side SiP (Free Air)

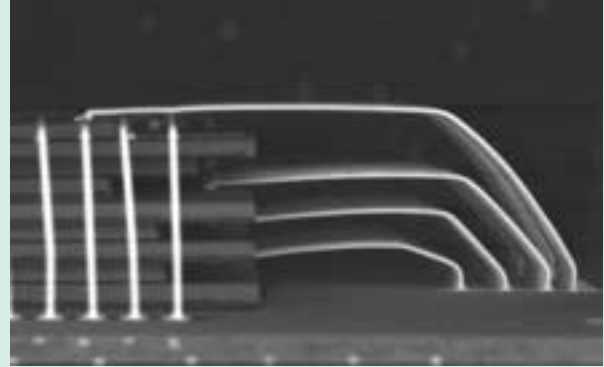
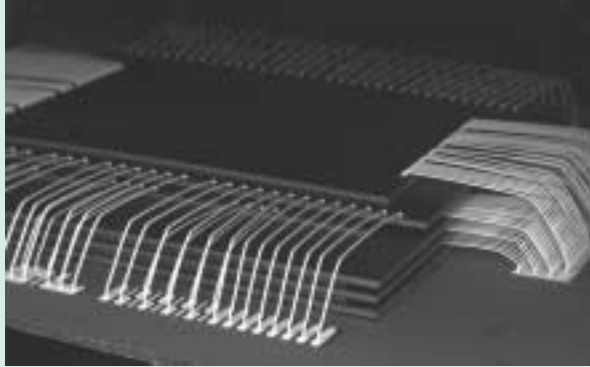


Thermal Flow for a Stacked SiP (Free Air)

Toshiba provides a solution for reducing the package's thermal impedance, based the package structure, chip size and substrate specifications. (θ_{JA} , θ_{JMA} , θ_{JC} and θ_{JB} can be calculated.)

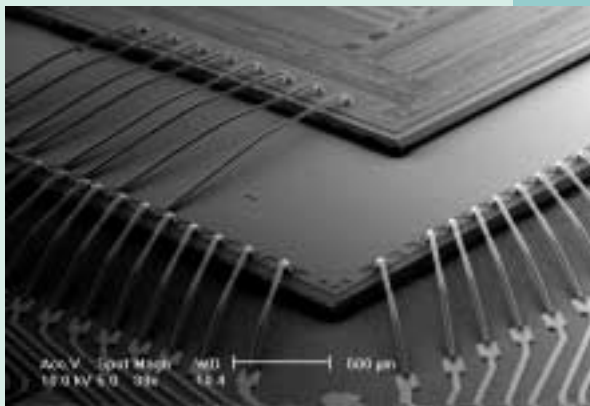
For space-constrained applications...

9-Layer MCP. (5 Die Stacked Die)



Toshiba's SiP solution fully leverages its advanced die backgrinding technology to allow up to 9 die stack.

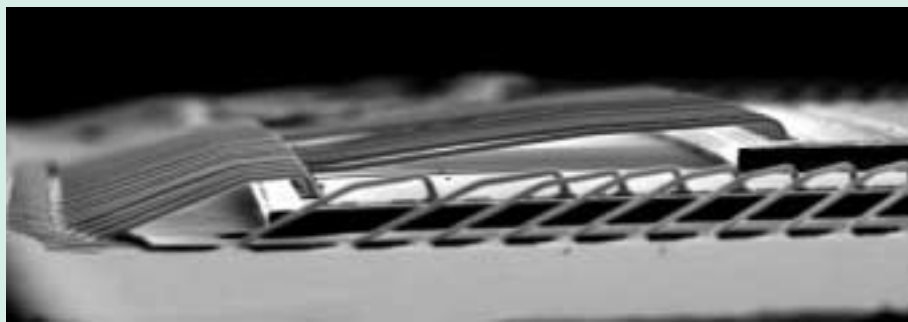
For height-constrained applications...



Ultra-Thin Stacked SiP
Chip thickness: 60 µm



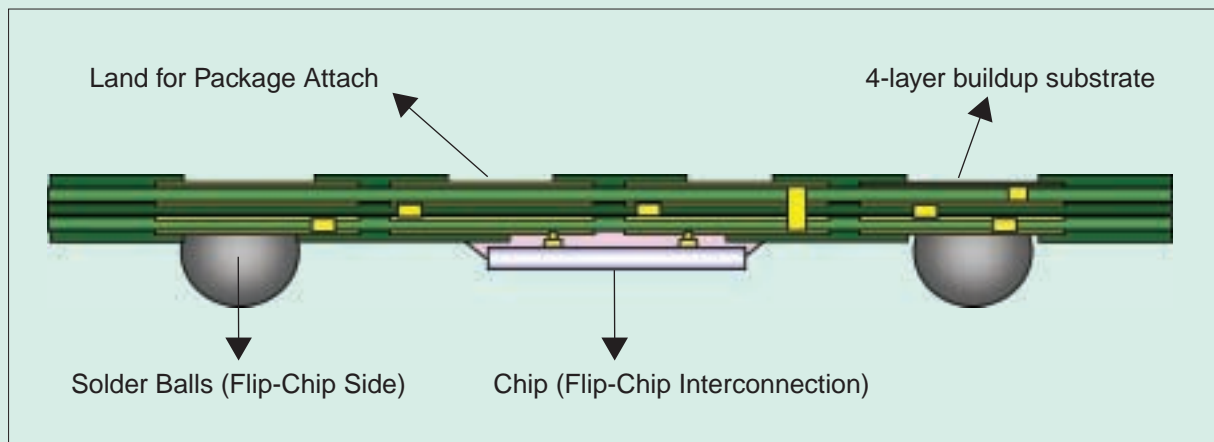
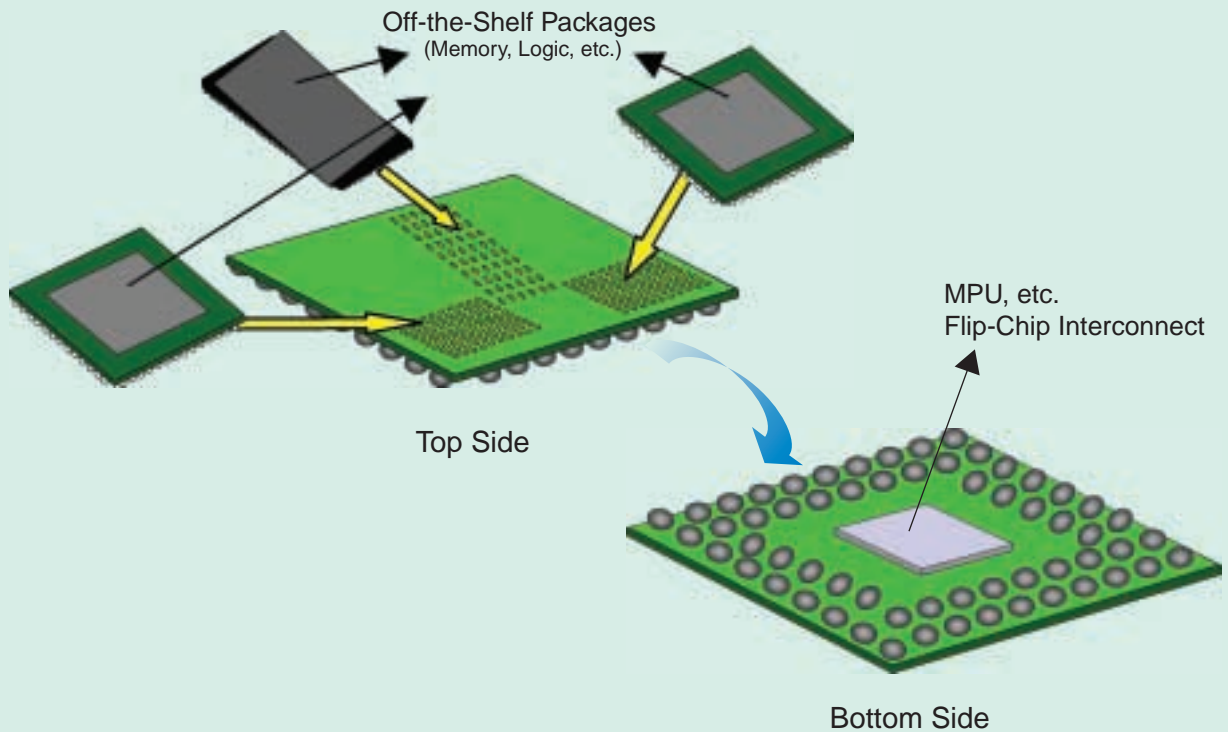
2-Layer Stacked SiP: Max.
Thickness = 0.55 mm



Low Loop Wire Bonding

Using off-the-shelf packages in package stacking...

Package-on-Package Stacking



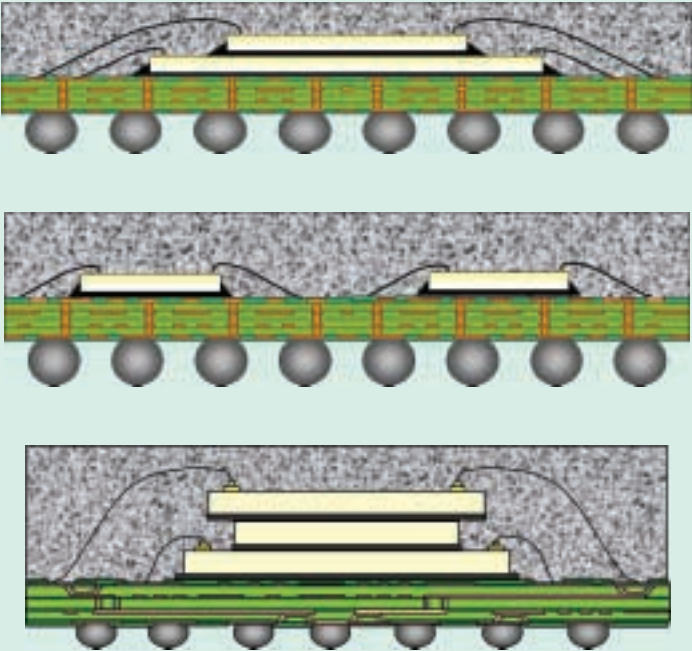
Toshiba provides package-on-package stacking solutions. This approach helps to combine off-the-shelf packages on top of a logic chip that constitutes a major part of your system.



Package Types

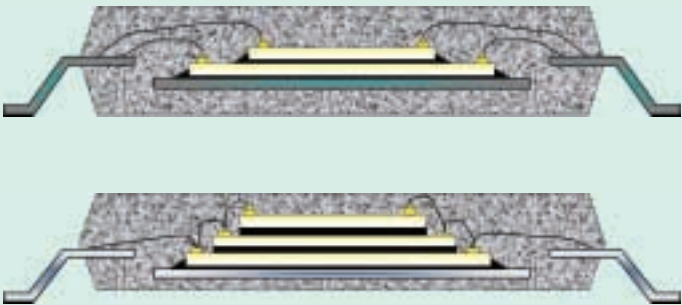
Laminate Packages

FBGA (Fine Pitch Ball Grid Array)
PBGA (Plastic Ball Grid Array)

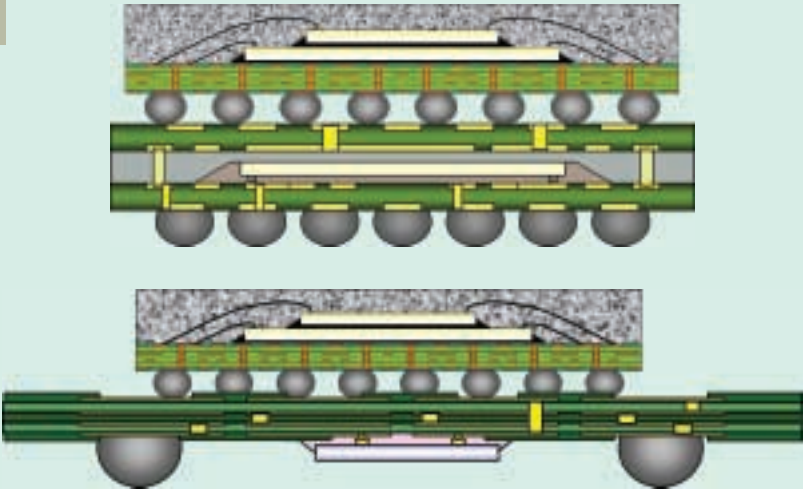


Leadframe Packages

QFP (Quad Flat Packages)
LQFP (Low-Profile Quad Flat Packages)
TSOP (Thin Small Outline Packages)

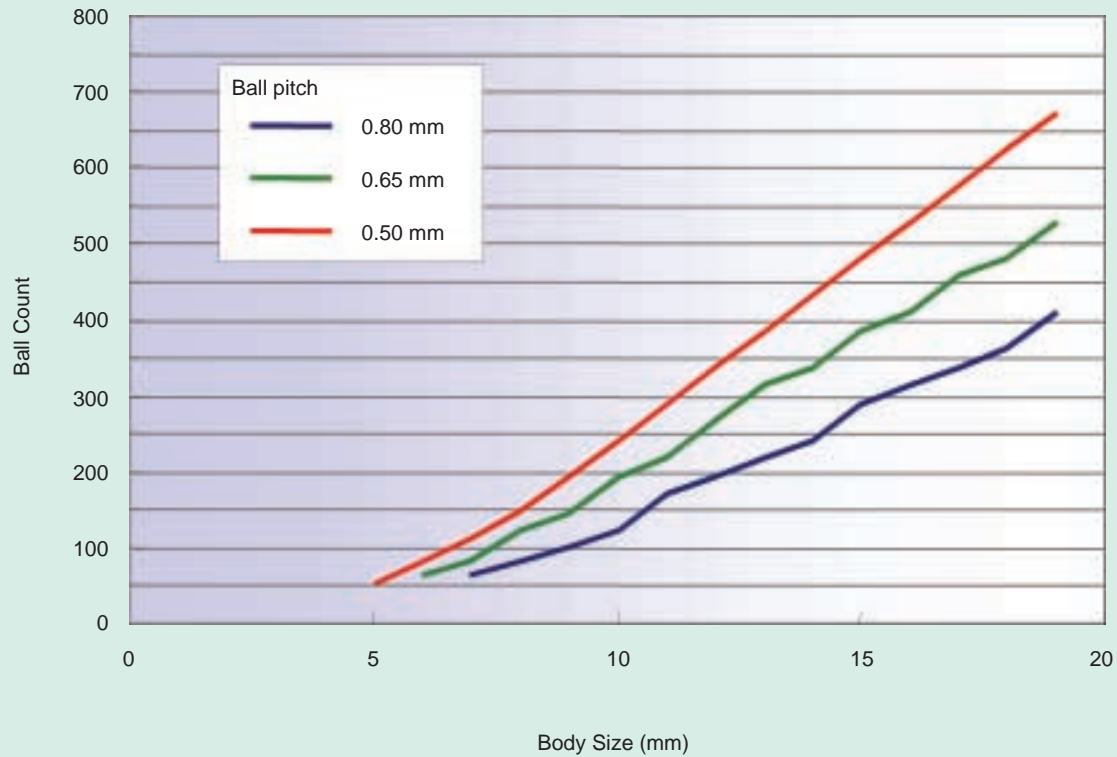


Package on Package



Package Body Sizes vs. Ball Counts

FBGA Standard Offerings



Body Size (mm)	0.80 mm	0.65 mm	0.50 mm
5 × 5	—	—	52
6 × 6	—	64	80
7 × 7	64	81	112
8 × 8	81	121	148
9 × 9	100	144	192
10 × 10	121	192	240
11 × 11	168	216	288
12 × 12	192	264	336
13 × 13	216	312	384
14 × 14	240	336	432
15 × 15	288	384	480
16 × 16	312	408	528
17 × 17	336	456	576
18 × 18	360	480	624

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