第 2 回配布資料

半加算器の VHDL 記述

```
library ieee;
use ieee.std_logic_1164.all;

entity half_adder is
  port (
    a, b : in std_logic;
    s, co : out std_logic);
end half_adder;

architecture arch of half_adder is
  signal w0, w1, w2: std_logic;
begin
  w0 <= a and b;
  w1 <= not w0;
  w2 <= a or b;
  s <= w1 and w2;
  co <= w0;
end arch;
```

全加算器の VHDL 記述

```
library ieee;
use ieee.std_logic_1164.all;

entity full_adder is
  port (
    a, b, ci: in std_logic;
    s, co: out std_logic);
end full_adder

architecture arch of full_adder is
  component half_adder
    port (
      a, b: in std_logic;
      s, co: out std_logic;
  end component;
  signal w0, w1, w2: std_logic;
begin
  co <= w1 or w2;
  i0: half_adder port map (co=>w1, s=>w0, a=>a, b=>b);
  i1: half_adder port map (co=>w2, s=>s, a=>w0, b=>ci);
end arch;
```

４ビット全加算器の VHDL 記述

```
library ieee;
use ieee.std_logic_1164.all;

entity adder4 is
  port (
    a, b: in std_logic_vector(3 downto 0);
    ci : in std_logic;
    s: out std_logic_vector(3 downto 0);
    co: out std_logic);
end adder4;

archtiecture arch of adder4 is
  component full_adder
    port (
      a, b, ci: in std_logic;
      s, co: out std_logic);
  end component;
  signal w0, w1, w2: std_logic;
begin
  i0: full_adder port map(co=>w0, s=>s(0), a=>a(0), b=>b(0), ci=>ci);
  i1: full_adder port map(co=>w1, s=>s(1), a=>a(1), b=>b(1), ci=>w0);
  i2: full_adder port map(co=>w2, s=>s(2), a=>a(2), b=>b(2), ci=>w1);
  i3: full_adder port map(co=>co, s=>s(3), a=>a(3), b=>b(3), ci=>w2);
end arch;
```

４ビット全加算器の VHDL 記述（動作記述）

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;

entity adder4 is
  port (
    a, b: in std_logic_vector(3 downto 0);
    ci : in std_logic;
    s: out std_logic_vector(3 downto 0);
    co: out std_logic);
end adder4;

architecture behv of adder4 is
begin
  process (a, b, ci)
    variable tmp: std_logic_vector(4 downto 0);
  begin
    tmp := ("0"&a) + ("0"&b) + ("0000"&ci);
    co <= tmp(4);
    s  <= tmp(3 downto 0);
  end process
end behv;
```

４ビット全加算器のテストベンチ VHDL 記述

```
library ieee;
use ieee.std_logic_1164.all;

entity test_adder is
end test_adder4;

architecture arch of test_adder4 is
  component adder4
    port (
      a, b: in std_logic_vector(3 downto 0);
      ci: in std_logic;
      co: out std_logic;
      s: out std_logic_vector(3 downto 0));
  end component
  for i0: adder4 use entity work.adder4(arch);
  signal a, b: std_logic_vector(3 downto 0);
  signal ci: std_logic;
  signal co: std_logic;
  signal s: std_logic_vector(3 downto 0);
begin
  i0: adder4 port map (a=>a, b=>b, ci=>ci, co=>co, s=>s);
  process begin
    a <= "0000"; b <= "0000"; ci <= '0';
    wait for 100ns;
    a <= "1010"; b <= "0101"; ci <= '0';
    wait for 100ns;
    a <= "1010"; b <= "0101"; ci <= '1';
    wait for 100ns;
    a <= "1111"; b <= "0001"; ci <= '0';
    wait for 100ns;
    wait;
  end process;
end arch;
```