第８回配布資料

ALU (Arithmetic & Logic Unit)

```vhdl
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

entity alu is
  port (
    a, b: in std_logic_vector(7 downto 0);
    opcode: in std_logic_vector(2 downto 0);
    x: out std_logic_vector(7 downto 0)
  );
end alu;

architecture arch of alu is
begin
  process (a, b, opcode)
    case opcode is
      when I_AND => x <= a and b;
      when I_OR  => x <= a or b;
      when I_NOT => x <= not a;
      when I_XOR => x <= a xor b;
      when I_ADD => x <= a + b;
      when I_SUB => x <= a - b;
      when I_ACC => x <= a;
      when I_DAT => x <= b;
      when others => x <= "XXXXXXXX";
    end case;
  end process;
end arch;

package alu_pack is
constant I_AND: std_logic_vector(2 downto 0) := "000";
...
end alu_pack;
```