第９回配付資料

同期リセットつきレジスタ

```
library ieee;
use ieee.std_logic_1164.all;

entity sync_reg8 is
  port (
    clk, rst: in std_logic;
    d: in std_logic_vector(7 downto 0);
    q: out std_logic_vector(7 downto 0)
  );
end sync_reg8;

architecture arch of sync_reg8 is
begin
  process (clk) begin
    if (clk'event and clk = '1') then
      if (rst = '0') then
        q <= "00000000";
      else
        q <= d;
      end if;
    end if;
  end process;
end arch;
```

非同期セットつきレジスタ

```
library ieee;
use ieee.std_logic_1164.all;

entity async_reg8 is
  port (
    clk, rst: in std_logic;
    d: in std_logic_vector(7 downto 0);
    q: out std_logic_vector(7 downto 0)
  );
end async_reg8;

architecture arch of async_reg8 is
begin
  process (clk, rst) begin
    if (rst == '0') then
      q <= "00000000";
    elseif (clk'event and clk = '1') then
      q <= d;
    end if;
  end process;
end arch;
```

単純なカウンタ

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;

entity count8 is
  port (
    clk, rst: in std_logic;
    q: out std_logic_vector(7 downto 0);
  );
end count8;

architecture arch of count8 is
  signal q_reg: std_logic_vector(7 downto 0);
begin
  process (clk) begin
    if (clk'event and clk = '1') then
      if (rst = '0') then
        q_reg <= "00000000";
      else
        q_reg <= q_reg + 1;
      end if;
    end if;
  end process;
  q <= q_reg;
end arch;
```