第６回配布資料

デコーダ（３ビット→８ビット デコーダ）(p.62)

```
library ieee;
use ieee.std_logic_1164.all;

entity dec is
  port (
    a: in std_logic_vector(2 downto 0);
    x: out std_logic_vector(7 downto 0)
  );
end dec;

architecture arch of dec is
begin
  process (a) begin
    case a is
      when "000"  => x <= "00000001";
      when "001"  => x <= "00000010";
      when "010"  => x <= "00000100";
      when "011"  => x <= "00001000";
      when "100"  => x <= "00010000";
      when "101"  => x <= "00100000";
      when "110"  => x <= "01000000";
      when "111"  => x <= "10000000";
      when others => x <= "XXXXXXXX";
    end case;
  end process;
end arch;
```

エンコーダ（８ビット→３ビット エンコーダ）(p.64)

```
library ieee;
use ieee.std_logic_1164.all;

entity enc is
  port (
    a: in std_logic_vector(7 downto 0);
    x: out std_logic_vector(3 downto 0)
  );
end enc;

architecture arch of enc is
begin
  process (a) begin
    if    (a(0) = '1') then x <= "1000";
    elsif (a(1) = '1') then x <= "1001";
    elsif (a(2) = '1') then x <= "1010";
    elsif (a(3) = '1') then x <= "1011";
    elsif (a(4) = '1') then x <= "1100";
    elsif (a(5) = '1') then x <= "1101";
    elsif (a(6) = '1') then x <= "1110";
    elsif (a(7) = '1') then x <= "1111";
    else                    x <= "0000";
    end if;
  end process;
end arch;
```

セレクタ(p.67)

```
library ieee;
use ieee.std_logic_1164.all;

entity sel is
  port (
    a, b, c, d: in std_logic;
    s: in std_logic_vector(1 downto 0);
    x: out std_logic
  );
end sel;

architecture arch of sel is
begin
  process (a, b, c, d, s) begin
    case s is
      when "00"   => x <= a;
      when "01"   => x <= b;
      when "10"   => x <= c;
      when "11"   => x <= d;
      when others => x <= 'X';
    end case;
  end process;
end arch;
```

コンパレータ(p.69)

```
library ieee;
use ieee.std_logic_1164.all;

entity cmp is
  port (
    a, b: in std_logic_vector(7 downto 0);
    gt, lt, eq: out std_logic;
  );
end cmp;

architecture arch of cmp is
begin
  process (a, b) begin
    gt <= '0';
    lt <= '0';
    eq <= '0';
    if (a > b) then
      gt <= '1';
    elsif (a < b) then
      lt <= '1';
    else
      eq <= '1';
    end if
  end proess;
end arch;
```

加算器（8 ビット加算器）(p.71)

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

entity add is
  port (
    a, b: in std_logic_vector(7 downto 0);
    ci: in std_logic;
    co: out std_logic;
    x: out std_logic_vector(7 downto 0)
  );
end add;

architecture arch of add is
begin
  process (a, b, ci)
    variable tmp: std_logic_vector(8 downto 0);
  begin
    tmp := ("0" & a) + ("0" & b) + ("00000000" & ci);
    co <= tmp(8);
    x <= tmp(7 downto 0);
  end process;
end arch;
```

シフタ(p.73)

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;

entity shift is
  port (
    a: in std_logic_vector(7 downto 0);
    d: in std_logic;
    n: in_std_logic_vector(2 downto 0);
    x: out std_logic_vector(7 downto 0);
  );
end shift;

architecture arch of shift is
begin
  process (a, d, n) begin
    if (d = '1') then x <= sh_left(a, to_integer(n));
    else x <= sh_right(a, to_integer(n));
    end if;
  end process;
end arch;
```

乗算器(p.74)

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;

entity mult is
  port (
    a, b: in std_logic_vector(7 downto 0);
    x: out std_logic_vector(15 downto 0);
  );
end mult;

architecture arch of mult is
begin
  process (a, b) begin
    x <= a * b;
  end process;
end arch;
```

パリティ・ジェネレータ(p.77)

```
library ieee;
use ieee.std_logic_1164.all;

entity parity is
  port (
    a: in std_logic_vector(7 downto 0);
    x: out std_logic;
  );
end parity;

architecture arch of parity is
  -- bit reduction xor
  function br_xor(a: std_logic_vector) return std_logic is
    variable tmp:std_logic := '0';
  begin
    for i in a'range loop
      tmp := tmp xor a(i);
    end loop
    return(tmp);
  end br_xor;

begin
  process (a) begin
    x <= br_xor(a);
  end_process;
end arch;
```