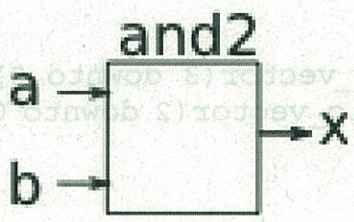
解答例

石川工業高等専門学校　電子情報工学科　システム設計演習　前期中間テスト　6月13日実施

番号	氏名　秋田純一

1．次のような入出力を持つ回路を VHDL で記述する際のエンティティ記述を完成させよ。なお回路の名称はブロック図の上に記されている。（10点×2）

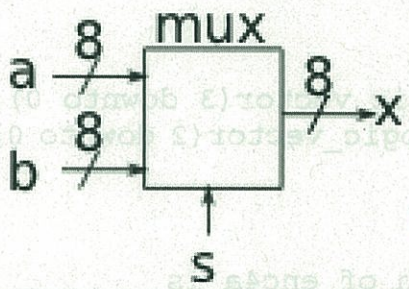
（1）



(10)

```
entity and2 is
    port(
      a, b: in std_logic;
      x : out std_logic
    );
end and2;
```

（2）



(10)

```
entity mux is
    port(
      a, b : in std_logic_vector
                    (7 downto 0);
      s    : in std_logic;
      x    : out std_logic
    );
end mux;
```

※文法ミス：各ポート

2．次のような回路の VHDL 記述で、それぞれの process 文のセンシティビティ・リスト(sensitivity list)に記述するべき信号名を、過不足なく記せ。（10×4点）

```
entity hoge1 is
  port (
    a, b, c, d, e, f: in std_logic;
    x: out std_logic
  );
end hoge1;

architecture arch of hoge1 is
begin
  process ([1]) begin
    case a is
      when '1'   => x <= b;
      when '0'   => x <= c;
    end case;
  end process;

  process ([2]) begin
    case d is
      when '1'   => x <= e and f;
      when '0'   => x <= not a;
    end case;
  end process;
end arch;
```

```
entity hoge2 is
  port (
    a, b: in std_logic_vector(1 downto 0);
    x: out std_logic
  );
end hoge2;

architecture arch of hoge2 is
begin
  process ([3]) begin
    case a is
      when "00"  => x <= '0';
      when "01"  => x <= '1';
      when others => x <= b(0);
    end case;
  end process;

  process ([4]) begin
    case b(0) is
      when '0'  => x <= a(0);
      when '1'  => x <= a(1);
    end case;
  end process;
end arch;
```

[1]　a, b, c　(10)

[2]　a, d, e, f　(10)

[3]　a, b(0)　(10)　「a, b」は△

[4]　a, b(0)　(10)　「a, b」は△

※順不同

3．次のようなVHDL記述の回路のそれぞれに、図１のような信号aを与えた場合に出力される信号x1とx2を図１中に示せ。なお図１の横軸は信号変化の時間経過である。（２０点×２）

```
library ieee;
use ieee.std_logic_1164.all;

entity enc4a is
  port (
    a: in std_logic_vector(3 downto 0);
    x1: out std_logic_vector(2 downto 0)
  );
end enc4a;

architecture arch of enc4a is
begin
  process (a) begin
    if    (a(0) = '1') then x1<= "100";
    elsif (a(1) = '1') then x1 <= "101";
    elsif (a(2) = '1') then x1 <= "110";
    elsif (a(3) = '1') then x1 <= "111";
    else x1 <= "000";
    end if;
  end process;
end arch;
```

```
library ieee;
use ieee.std_logic_1164.all;

entity enc4b is
  port (
    a: in std_logic_vector(3 downto 0);
    x2: out std_logic_vector(2 downto 0)
  );
end enc4b;

architecture arch of enc4b is
begin
  process (a) begin
    x2 <= "000";
    if    (a(3) = '1') then x2<= "111";
    elsif (a(2) = '1') then x2 <= "110";
    elsif (a(1) = '1') then x2 <= "101";
    elsif (a(0) = '1') then x2 <= "100";
    end if;
  end process;
end arch
```

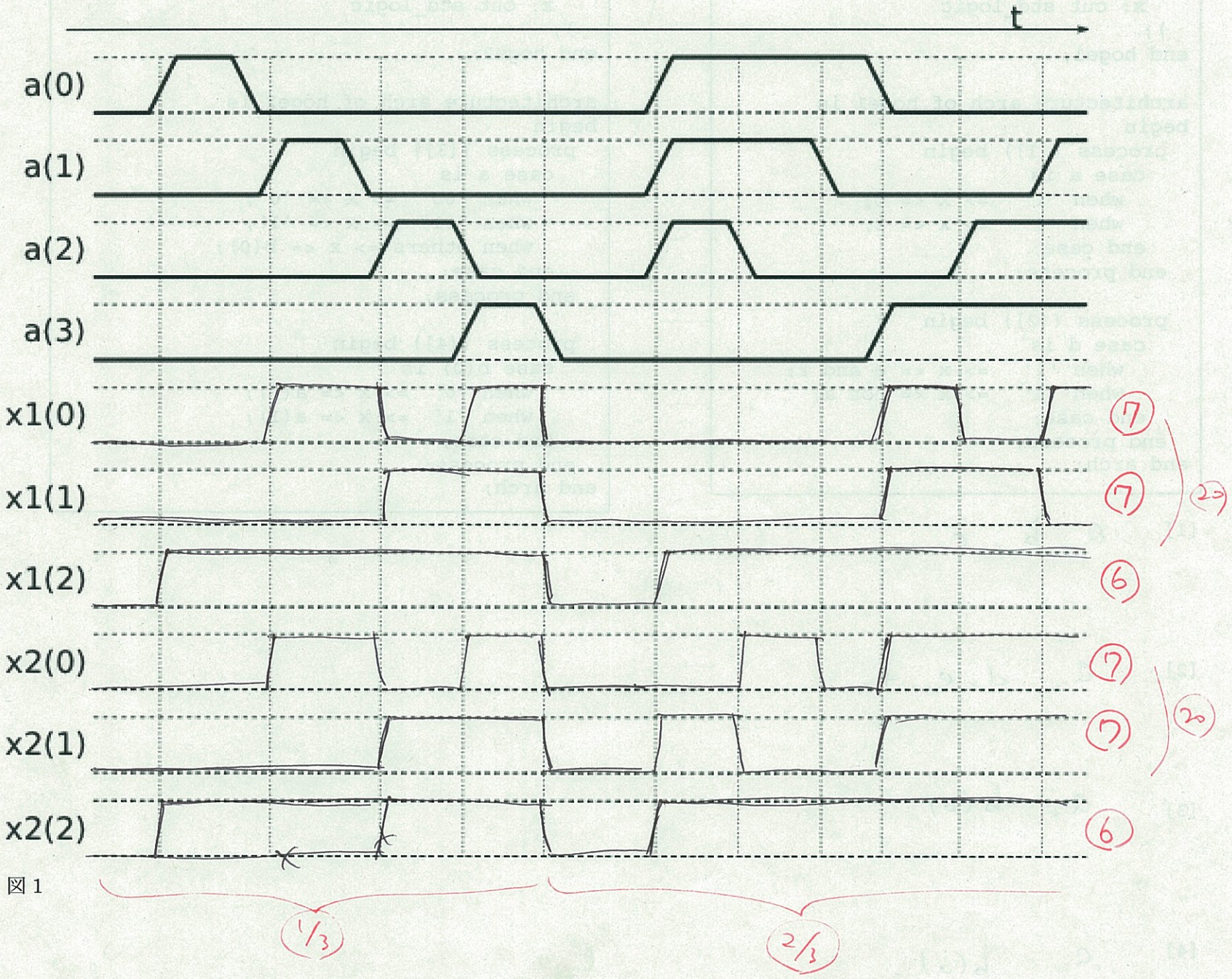


図１