Chapter 2

Power Reduction Methodologies for Image Sensors and CMOS Circuits

In this chapter, the problems of power consumption in image sensors and CMOS circuits will be discussed. In section 2.1, the models of power consumption in conventional image sensors will be described. In the following section 2.2 and section 2.3, the probabilistic models of power consumption in CMOS combinational logics and sequential circuits will be described. It will be also discussed the power reduction methodologies for CMOS combinational logics and sequential circuits with maintaining the performance in these sections.

2.1 Power Consumption Modeling of Image Sensors

Figure 2.1 describes the typical architecture of CCD transfer image sensors. Image signals are converted to charge in each photo detector, shown as squares in Figure 2.1, and the charge is carried to the vertical transfer CCDs and horizontal transfer CCDs outside to the image sensor.

The clock signals provided to each CCD are usually multi-phase clock signals, and their swings are often very large compared with the CMOS logic circuits. For

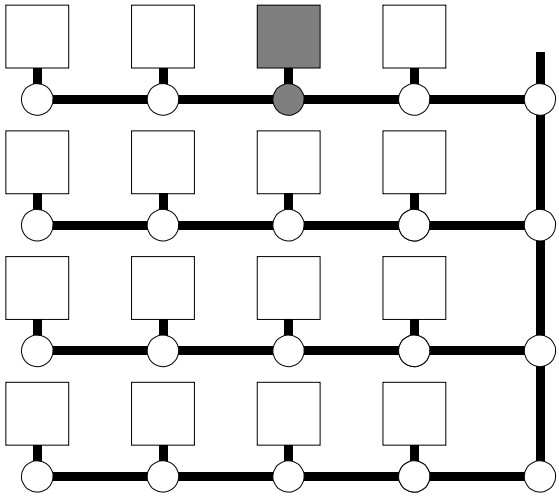


Figure 2.1: The simplified model of CCD transfer image sensors. (The square presents the photo detector, and the circle presents the transfer CCD.)

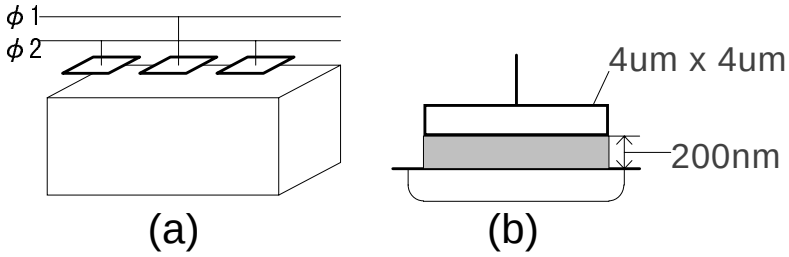


Figure 2.2: Model structure of CCD transfer gate. (a)a part of transfer line, (b)example size of unit CCD transfer gate.

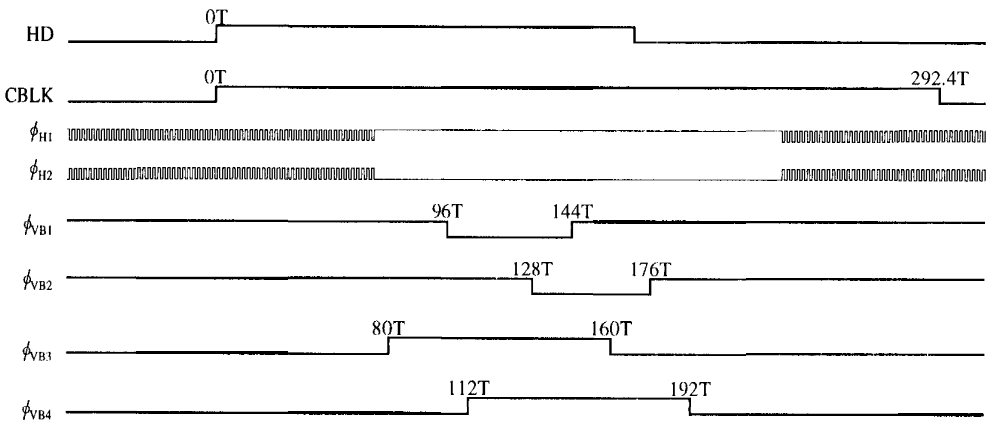


Figure 2.3: Example of multi-phase clocks for CCD devices (From [15])

example, the voltage swing of -7V to 0V is provided for vertical transfer CCDs, and 0V to $+5$V for horizontal transfer CCDs. Such a high clock voltage is needed because of the large size of devices, which is not easy to be scaled down to keep the charge transfer efficiency. (On the other hand, the size of MOSFETs in conventional CMOS logics can be reduced by the advanced fabrication technology, and it results in both power and delay reduction[14].)

The multi-voltage and multi-phase clock signals, for example as shown in Figure 2.3, should make the control circuits more complex.

It is notable that the clock signals are always provided to all transfer CCDs, and the number of transfer CCDs is quite large, it is almost same to the number of pixels, for example about 350,000 for VGA resolution image sensors.

Figure 2.4 shows the model structure of CCD transfer gates in image sensors. Assuming that the vertical and the horizontal number of pixels are both equal to n, the number of vertical and horizontal transfer CCD, n_v and n_h, respectively, are equal to $n_v = n^2$ and $n_h = n$, respectively. In case of scanning pixels, the transfer clocks for vertical CCDs are provided n times, while the transfer clocks for horizontal CCD are provided n^2 times. The total number of clocks provided for vertical and horizontal CCDs are equal to $2n^3$, and the power consumption in transfer CCDs is expected to be proportional to $O(n^3)$, which will be one of the most important problems in mega-pixel CCD image sensors.

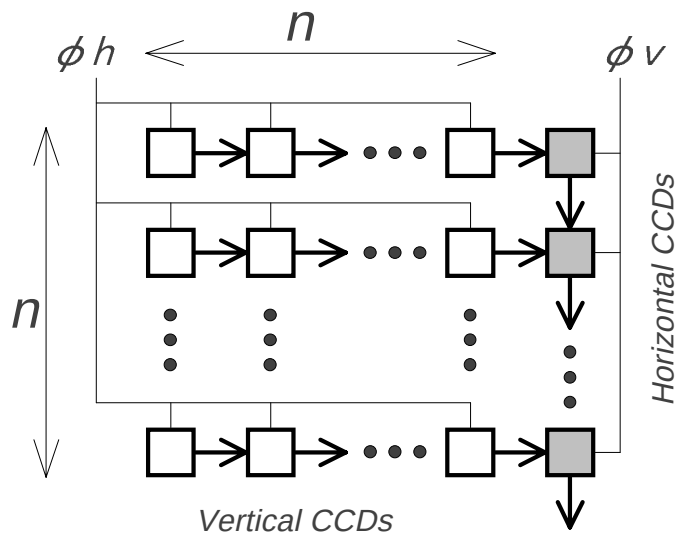


Figure 2.4: Model of CCD image sensor

Discussed in above, the reasons of increasing power consumption of CCD image sensors are follows.

- Clock signals are always provided to the all transfer CCDs. The number of transfer CCDs is almost same to the number of pixels.
- Voltage of clock signals can not be reduced because of the large size of devices. It is difficult to reduce the size of devices to keep the transfer efficiency.

The another type image sensor is based on memory-like architecture as shown in Figure 2.5. The non-CCD image sensor of this architecture has the advantages as follows.

- Just the address lines to the pixels being scanned are activated, and the most of address lines are not activated.
- The row and column decoders are combinational logics, and it can be "scaled down" in order to reduce power consumption. The driving voltage for each pixel can be kept to be equal to the supply voltage of decoder logics, which is lower than that of CCD image sensors.

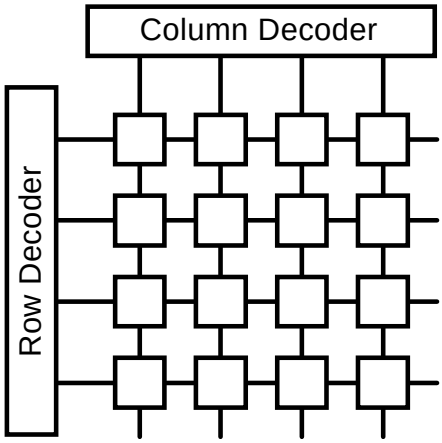


Figure 2.5: Model of non-CCD image sensor. (The squares represents the photo detectors, and the horizontal and vertical lines acrossing the photo detectors are address lines.)

In spite of the switching noise problem, the non-CCD image sensors (they are often called as "CMOS sensors") are expect to be a low power image sensor compared with CCD image sensors.

2.2 Models of Power Consumption in CMOS Combinational Logics and Its Reduction

In non-CCD type image sensors seen in previous section, the conventional logic elements, such as combinational logic gates and sequential circuits including flip-flops are used in non-CCD image sensors for signal scanning circuits. In this section, the power consumption modeling of CMOS combinational logics are described. It is also discussed the power reduction methodologies for combinational logics with keeping circuit function and circuit performance at the design step after logic synthesis.

2.2.1 Probabilistic power model of CMOS combinational logics

Here we assume that the input signals for combinational logic have the following characteristics.

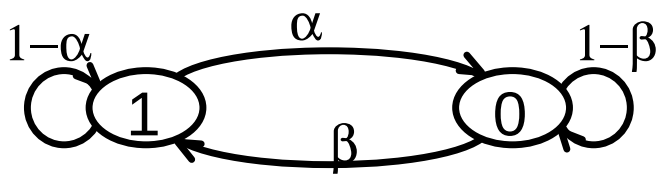


Figure 2.6: Definition of probabilistic parameters, (α, β).

- Input signals change synchronously with the system clock.
- Input signals change probabilistically concerning with the value in the previous cycle. (Markov chain)
- Input signals change independently.

Letting α and β to be conditional probabilities of "0" to "1" and "1" to "0", respectively as shown in Figure 2.6, the probabilities from "0" to "0" and "1" to "1" are equal to $(1-\alpha)$ and $(1-\beta)$, respectively. Here we call the pair of (α, β) as the probabilistic parameters of input signal. Assuming the stable state of input signals, the probability of input signal being "0", P_0 is derived from the following equation.

$$P_0 = P_0(1-\alpha) + (1-P_0)\beta \tag{2.1}$$

From the Equation (2.1), the P_0 and the probability of input being "1", P_1 are derived as follows.

$$P_0 = \frac{\beta}{\alpha+\beta} \tag{2.2}$$

$$P_1 = \frac{\alpha}{\alpha+\beta} \tag{2.3}$$

The load capacitances of logic circuits are charged or discharged along to the input signals, which are the most part of the power consumption of CMOS logics. For example, 2 input NAND gate can be simplified as shown in Figure 2.7. It has two load capacitances, the load capacitance C_L and the internal node capacitance C_i. Assuming that the probabilistic parameters of input x and y are (α_x, β_x) and (α_y, β_y), respectively, the stable probabilities for all combinations of input signals

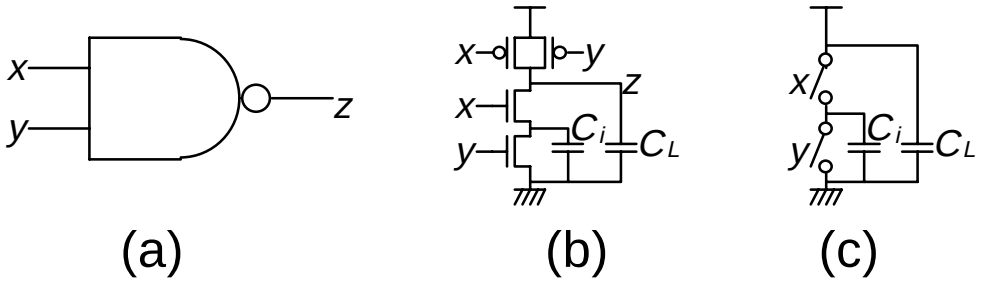


Figure 2.7: Models of 2 input NAND gate. (a)gate model, (b)transistor model, (c)switch model.

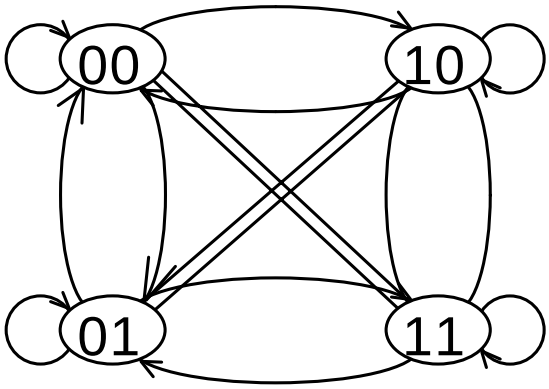


Figure 2.8: Transition diagram of two inputs.

are derived as follows.

$$P_{00} = \frac{\beta_x}{\alpha_x + \beta_x} \cdot \frac{\beta_y}{\alpha_y + \beta_y} \tag{2.4}$$

$$P_{10} = \frac{\alpha_x}{\alpha_x + \beta_x} \cdot \frac{\beta_y}{\alpha_y + \beta_y} \tag{2.5}$$

$$P_{01} = \frac{\beta_x}{\alpha_x + \beta_x} \cdot \frac{\alpha_y}{\alpha_y + \beta_y} \tag{2.6}$$

$$P_{11} = \frac{\alpha_x}{\alpha_x + \beta_x} \cdot \frac{\alpha_y}{\alpha_y + \beta_y} \tag{2.7}$$

Here P_{XY} means the probability of $x = X$ and $y = Y$.

Using these probabilities, the all transition probabilities between two combinations of inputs, as shown in Figure 2.8 can be derived. For example, the probability of transition from $(x, y) = (0, 1)$ to $(x, y) = (1, 1)$ is equal to the product of P_{01} and

the conditional probability of $x = 0$ to $x = 1$, α_x and $y = 1$ to $y = 1$, $1 - \beta_y$, as follows.

$$P_{01\to 11} = P_{01}\alpha_x(1-\beta_y) = \frac{\beta_x}{\alpha_x+\beta_x}\frac{\alpha_y}{\alpha_y+\beta_y}\alpha_x(1-\beta_y)$$

It also can be derived the probabilistic parameters of output z, (α_z, β_z) along to the transition diagram of output node z, as follows.

$$\alpha_z = 1-(1-\beta_x)(1-\beta_y) \tag{2.8}$$

$$\beta_z = \{P_{00}(1-\alpha_x\alpha_y) + P_{10}(1-\alpha_y+\beta_x\alpha_y) + P_{01}(1-\alpha_x+\alpha_x\beta_y)\} \\ / (P_{00}+P_{01}+P_{10}) \tag{2.9}$$

In the switch level model shown in Figure 2.7, both load capacitances have two states; charged state ("1") and discharged state ("0"). The states of load capacitances C_L and C_i change between "1" and "0", and it is easy to be describe the probabilistic parameters of charging/discharging each load capacitance, $(\alpha_{C_L}, \beta_{C_L})$ and $(\alpha_{C_i}, \beta_{C_i})$ as follows.

$$\alpha_{C_L} = \alpha_z \tag{2.10}$$

$$\beta_{C_L} = \beta_z \tag{2.11}$$

$$\alpha_{C_i} = \frac{P_{00}^{(0)}(\alpha_x - \alpha_x\alpha_y) + P_{01}\alpha_x\beta_y + P_{11}(\beta_y - \beta_x\beta_y)}{P_{00}^{(0)} + P_{01} + P_{11}} \tag{2.12}$$

$$\beta_{C_i} = 1-\alpha_y \tag{2.13}$$

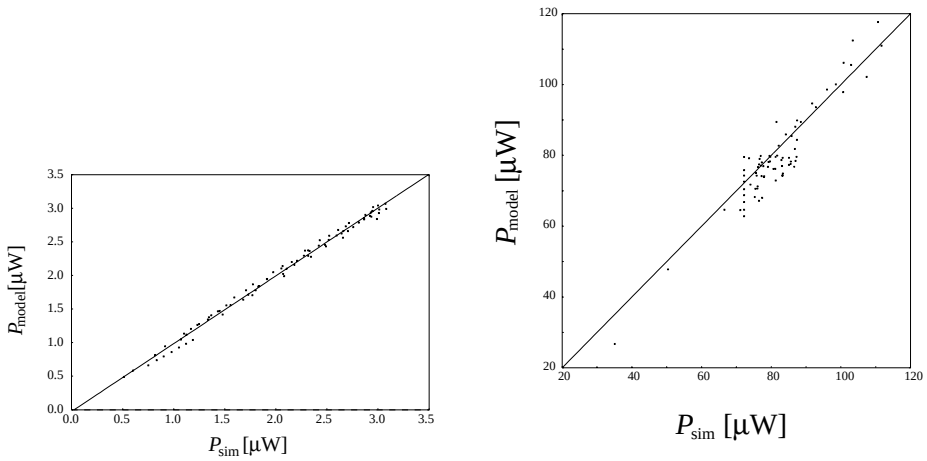
Here $P_{00}^{(0)}$ is the probability of inputs are both "0", with the discharged state of C_i, which is floating in this case, as follows.

$$P_{00}^{(0)} = \frac{P_{01}(1-\alpha_x)\beta_y + P_{11}\beta_x\beta_y}{\alpha_x+\alpha_y-\alpha_x\alpha_y} \tag{2.14}$$

The probabilistic parameters of load capacitances give the probabilities of charging load capacitances, $\overline{N_{C_L}}$ and $\overline{N_{C_i}}$, respectively, as the product of the probability of state "0" and the transition from "0" to "1", as follows.

$$\overline{N_{C_L}} = \frac{\alpha_{C_L}\beta_{C_L}}{\alpha_{C_L}+\beta_{C_L}} \tag{2.15}$$

$$\overline{N_{C_i}} = \frac{\alpha_{C_i}\beta_{C_i}}{\alpha_{C_i}+\beta_{C_i}} \tag{2.16}$$



(a) (b)

Figure 2.9: Calculated power by probabilistic model, Pmodel and `spice` simulation, P_{sim}. (a)2-input NAND gate and (b)1-bit full adder

Using these probabilities, the expectation of power consumption per one system clock cycle, $\overline{P}$ is described as follows.

$$\overline{P} = f\{\overline{N_{C_L}} C_L V_{dd}^2 + \overline{N_{C_i}} C_i V_{dd}(V_{dd} - V_T)\} \tag{2.17}$$

Here f is the system clock frequency, V_{dd} is the supply voltage, and V_T is the threshold voltage of n-channel MOSFETs.

This probabilistic model of power consumption can be extended for a large logic circuits containing many logic gates by assuming that the probabilistic parameters of a input signal are equal to those of the output signals connected to it.

The accuracy of this probabilistic model is checked by `spice` simulation, as shown in Figure 2.9. P_{sim} and P_{model} represent the power consumption calculated from `spice` simulation results[16], and from the probabilistic model by Equation (2.17), respectively. Simulations for both 2-input NAND gate and 1-bit full adder, containing 9 NAND gates shown in Figure 2.10, are shown in Figure 2.9(a) and 2.9(b), respectively. Figure 2.9(b) indicate a small difference between the power calculated by `spice` simulation and that of the probabilistic model in case of 1-bit full adder. The reason is that signals of each gate in the circuits are not always independent each other.

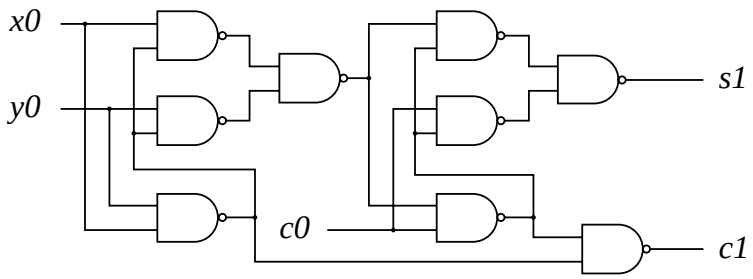


Figure 2.10: Circuit of 1-bit full adder

2.2.2 Power reduction methodologies for CMOS combinational logics

Figure 2.7 gives the hints of reducing power consumption without changing logic function of 2-input NAND gate. The inputs x and y are symmetric logically, though they are asymmetric topologically. The charge and discharge for load capacitance C_L will happen depending on the state of output signal, but charge and discharge for internal capacitance will depend on the state of C_i, since C_i will be opened when $x = y = 0$ and keeps the previous state. This situation will depend on whether input signals S_x and S_y are connected to the input terminals x and y, respectively, or connected to the input terminals y and x, respectively, though these two cases give the identical logic function of 2-input NAND gate.

We can choice the optimal input assignment by comparing the expectation of power calculated from the probabilistic model.

For example, we carried out the simulation for the 1-bit full adder shown in Figure 2.10, which has 9 2-input NAND gates and tree inputs; x_0, y_0 and c_0. There are $2^9 = 512$ possible input signal assignments for all NAND gates, and the maximum power consumption, $U_{\max}$ and the minimum power consumption, $U_{\min}$ in all possible assignments are shown in Figure 2.11. Here we assume that C_L=40fF, C_i=20fF, $\alpha_{x_0} = \beta_{x_0} = 0.1$, $\alpha_{y_0} = \beta_{y_0} = p_{y_0}$ and $\alpha_{c_0} = \beta_{c_0} = p_{c_0}$. The result shows that there are the ratio of $U_{\max}/U_{\min}$ of 1.74 in maximum and 1.10 in minimum, and this implies that the power consumption of 1-bit full adder can be reduced about 40% in maximum by the optimum input assignment, without the modification of logic function.

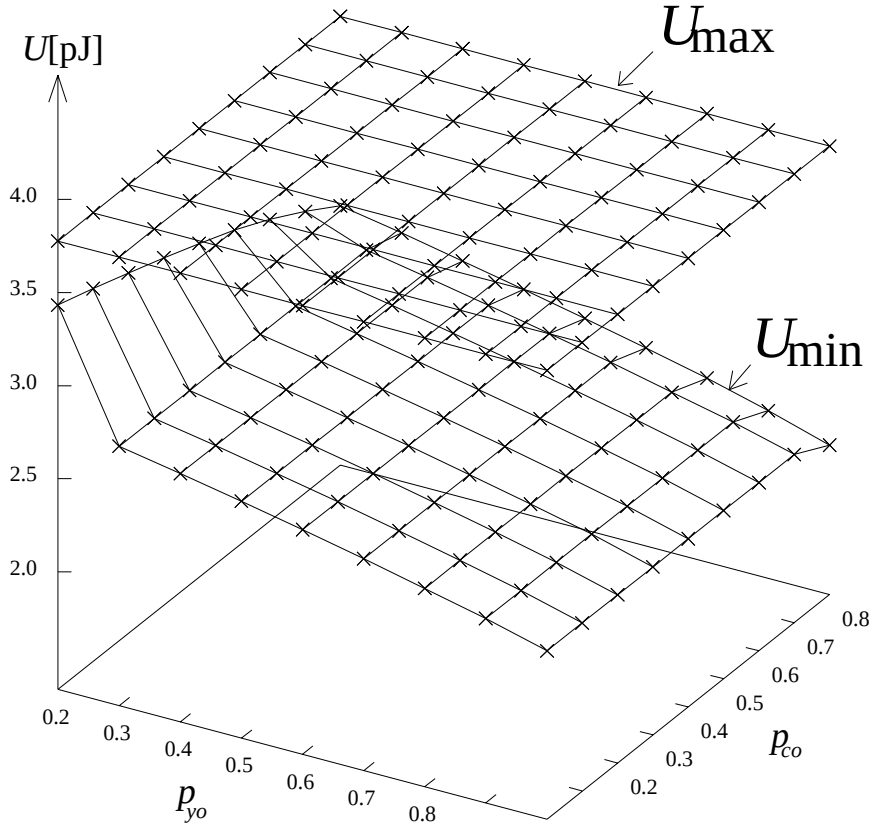


Figure 2.11: Maximum and minimum of power consumption of 1-bit full adder for various probabilistic parameters of input y_0 and c_0.

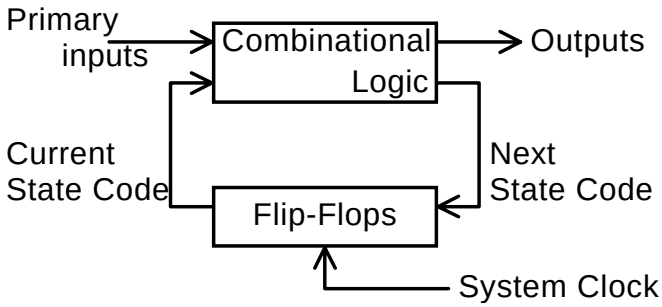


Figure 2.12: Architecture of finite state machine (FSM).

2.3 Models of Power Consumption in CMOS Sequential Circuits and Its Reduction

In this section, the power consumption modeling of CMOS sequential circuits are described. It is also discussed the power reduction methodologies for sequential circuits by the state code assignments for each state.

2.3.1 Probabilistic power model of CMOS sequential circuits

Here we consider the sequential circuit as the finite state machine (FSM), as shown in Figure 2.12. The most part of CMOS circuits' power consumption is the dynamic power consumption, caused by charging and discharging load capacitance, as discussed in the previous section. The dynamic power consumption of sequential circuits consists of two parts; the power consumption of flip-flops, P_{FF} and that of combinational logics, P_{logic}. The power consumption of flip-flops is composed of two parts; the power consumption by charging and discharging the load capacitance of flip-flops based on the state transition, $P_{\mathrm{FF(load)}}$ and that by charging and discharging system clock lines, $P_{\mathrm{FF(clock)}}$.

$P_{\mathrm{FF(load)}}$ depends on the number of flip-flops whose outputs have changed, while $P_{\mathrm{FF(clock)}}$ is almost constant for every clock cycle, whether the all or no flip-flops have made transition.

This fact implies that there is a possibility of reducing power consumption by load capacitance, $P_{\mathrm{FF(load)}}$, since the way to assign of the binary state code for each

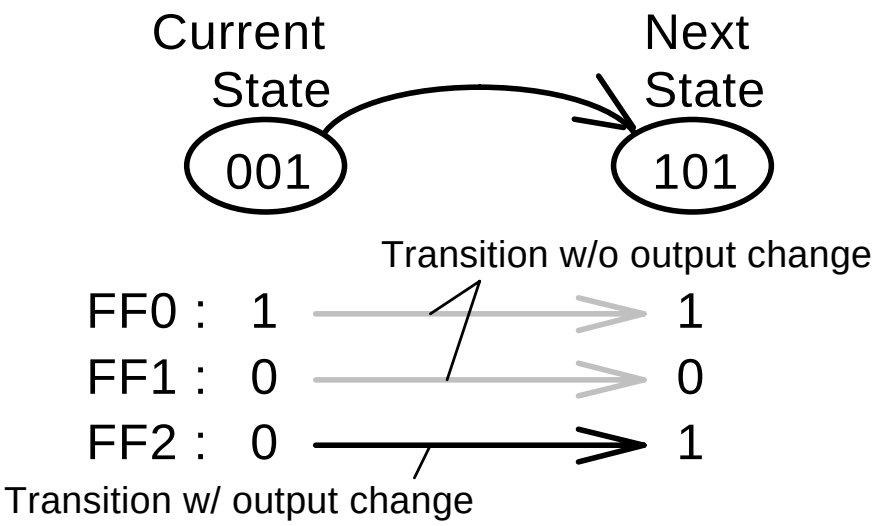


Figure 2.13: Charging and discharging load capacitance at every state transition.

state in the transition diagram is not unique; it is often determined to minimize the complexity of combinational logics.

Assuming that the conditional probabilities of the transition from state i to state i, $\overline{p}_{i,j}$ are known, the probabilities of occupying state i at each cycle, q_i should satisfy the following equation.

$$q_i = \sum_{j=1}^{N} \overline{p}_{i,j} \cdot q_j \tag{2.18}$$

Here N is the number of states in the transition diagram. Using the matrix $\overline{\boldsymbol{P}}$, whose (i,j) element is $\overline{p}_{i,j}$ and the vector $\boldsymbol{q}$, whose i element is q_i, the Equation (2.18) can be described as follows.

$$\boldsymbol{q} = \overline{\boldsymbol{P}}\boldsymbol{q} \tag{2.19}$$

The solution of Equation (2.19) under the condition of $\sum q_i = 1$ gives the state probability of each state, q_i. The product of q_j and $\overline{p}_{i,j}$, $p_{i,j} = \overline{p}_{i,j} \cdot q_i$ gives the transition probability at each clock cycle.

It is notable that the number of flip-flops whose output have changed at clock cycle is equal to the Hamming distance, $d_{i,j}$ between two state. The expectation of the number of flip-flops whose output have changed at clock cycle should be equal to the mean Hamming distance, $\overline{d}$, as is described as follows.

$$\overline{d} = \sum_{i=1}^{N} \sum_{j=1}^{N} p_{i,j} \cdot d_{i,j} \tag{2.20}$$

This $\overline{d}$ is expected to be as an index of the power consumption in flip-flops.

2.3.2 Power reduction methodologies for CMOS sequential circuits

The simple methodology of reducing P_{FF} in the sequential circuits is to find the binary state code assignment for each state which minimizes the mean Hamming distance, $\overline{d}$. There are $N!$ possible assignments of state codes for all N states, and it is undesirable to try the all possible assignments to find the assignment minimizing $\overline{d}$ for N states in practical design.

The alternative way to find the optimal state code assignment is the following heuristic algorithm.

1. calculate transition probabilities, $p_{i,j}$ and add $p_{i,j}$ and $p_{j,i}$, as $\tilde{p}_{i,j}$.

2. sort $\tilde{p}_{i,j}$ in order.

3. assign "0"(decimal) and "1"(decimal) for state i and j whose $\tilde{p}_{i,j}$ is the largest.

4. assign to the state i whose state code has not assigned yet, as one of the available state codes whose Hamming distance from state j is minimum, in order of $\tilde{p}_{i,j}$.

The simulation results shows that this heuristic algorithm can give the optimal assignment, with the error of about 4% against the optimum assignment by the exhaustive method, with the calculation time proportional to about $O(N^3)$ against about $O(N!)$ of the exhaustive method.

The simulation results of power consumption and the number of gates in combinational logics by this heuristic assignment compared with both the random assignment and the assignment aiming to minimize the complexity of the combinational logic[17] are shown in Table 2.1. The results shows about -10% power reduction against the conventional assignment for minimize logic complexity, and the number

	compared with	
	random assignment	logic minimize assignment
Power in flip-flops	-40%	-30%
Power in combinational logic	—	-11%
Total Power	—	-10%
# of gates	—	$+11\%$

Table 2.1: The comparison of power in each part and the number of gates by the assignment for minimum $\overline{d}$.

of gates in combinational logic increase about 10%, but the total increase of hardware costs will be smaller than this case, since the number of flip-flops is equal in each assignments.

2.4 Summary and Conclusion

In this chapter we discussed the power consumption in image sensors, both CCD sensors and "CMOS" sensors. This chapter also has described the probabilistic model of power consumption of both the combinational logics and the sequential circuits. It is shown that these models are adequate to analytically express the expectation of power consumption. It is also proposed the methodologies to reduce power consumption of both the combinational logics and the sequential circuits without modifying the designed functions. The efficiency of power reduction in the combinational logics is up to about -30% against the conventional random input signal assignment. The efficiency of power reduction in the sequential circuits is up to about -10% against the conventional assignment aiming to minimize the complexity of combinational logics.