Chapter 7

Conclusions

The followings are the conclusions through this thesis.

Chapter 2

The power consumption in CCD image sensor is estimated as proportional to the cubic of the number of pixels in line, which will be one of the most serious problems in mega-pixel CCDs.

The probabilistic model of power consumption for both combinational logics and sequential circuits are described.

It is also described the power reduction methodologies for both combinational logics and sequential circuits without modification of their function.

The power consumption of combinational logics, 1 bit full adder as an example, is expected to be reduced up to -30% by optimum input assignment for logically symmetric input terminals.

The power consumption of sequential circuits is expected to be reduced up to -10% by the binary state code assignment minimizing the mean number of transition at each clock cycle, against the conventional state code assignment minimizing the complexity of combinational logics. In this case, the number of transistors in combinational logics increases about 10% by minizing power consumption against minizing the complexity of combinational logics, while the total number of transis-

tors increase less than 10%, since the number of flip-flops is the same.

Chapter 3

A method of using tree structure for image signals is proposed, which is effective especially for the image containing many 0s by skipping redundant scan steps for the large area of 0s.

It is also derived that the optimal number of branches in the tree structure is 4, which we call "1:4 tree structure". The expectation of code length using 1:4 tree structure is shorter than that of the raster scan in case of less than quarter of the pixels are "1" in random white noise image, but in the practical image containing about half of "1" pixels can be scanned by 1:4 tree scan with the shorter code length than that of the raster scan.

It is also indicated that the code length by the scan using 1:4 tree structure is shorter than that of run-length compression, especially in case of containing many white pixels.

The methodology for decoding the 1:4 tree code is also described, where the partially decoded images represent the rough images corresponding to the current level of 1:4 tree structure.

Chapter 4

Some concepts and implementations are described for the applications of 1:4 tree sensor for various adaptivities of images as our eyesight has, and the algorithms used in movie compression, and visual tracking system.

The spatial adaptivity for scanning images is implemented by 1:4 tree scan with stopping the scan steps to the lower level, since the sub-areas corresponding to the nodes in the lower level represent the part of image with the higher spatial resolution. The selection whether the rough scan or the detail scan for each sub-area should be executed, is determined according to the interests for it. One of the criteria determining the spatial resolution for each area is the partial uniformity of image,

and the detail scan is executed for the sub-area with low uniformity, while the rough scan is executed for the sub-area of high uniformity. This scan method indicates one possibility of compressing images with maintaining the quality of image.

It is also described the intensional adaptivity for image signals using 1:4 tree structure, since the charge time of junction capacitance by photo current is concerned with the light intensity. The spatial distribution of the pixel whose output voltage reaches to the threshold voltage at each charge time, gathers spatially, which is the case that 1:4 tree scan can be executed efficiently.

The applications of 1:4 tree scan for two important algorithms used in movie compression, inter-frame difference and motion compensation, are described.

The 1:4 tree scan is used for the scan of flag indicating the pixels has a effective difference in successive two frames, which is the case that 1:4 tree structure can scan efficiently, and the analog value of difference can be read out by the other signal path.

The motion compensation within one pixels, which is expected to be suitable assuming high frame rate, can be implemented by adding the interconnections among neighbor pixels and the selector of them to each pixel. It is also notable that the motion compensation using this algorithm can be executed for any size of sub-areas, since the node automata has the mean value of its lower sub-areas.

It is also described the visual tracking algorithm using 1:4 tree structure, which can scan just for the areas containing moving objects with masking the other areas.

Chapter 5

The implementations of 1:4 tree structure in CMOS circuit are described. In the designed node automata, the clock signals are provided just along the scan path, which is expected to be suitable for low power operation. The two dimensional layout of node automata and pixels that can be extended for any number of levels are described, by placing the magnified cross-shaped node automata for the higher level, which is also suitable for minizing the signal delay.

The alternative implementation of 1:4 tree structure is also described, by plaicing

address decoders indicating the pixels to be scanned outside the pixel plain. The 1:4 tree sensor using this architecture is expected to achieve the higher fill factor and higher integration of pixels in image sensor.

The architecture of decoder for 1:4 tree code is also described, which is implementing the identical address decoders and controllers used in the 1:4 tree sensor using external address decoders.

The circuits of pixels are also described, which implement taking inter-frame difference, and gray scale scan considering charge-up time by photo current.

It is also described the concept of light-powered 1:4 tree sensor for ultra low power operation.

Chapter 6

The design and evaluation of 1:4 tree sensors using node automata are described, for both prototype system using FPGAs and full custom chip using 1.5μm CMOS technology is discussed. The designed chip contains 32×32 pixels in 7.2mm$\times$7.2mm chip, and its power consumption at each scan step is expect to be proportional to the edge size, which is smaller enough than CCD image sensors in mega-pixel sensors.

The photo current of photo diodes is also measured, and the photo current of the photo diode with $36\mu\text{m} \times 100\mu\text{m}$ is about 1μA, and it is proportional to both light intensity and area of photo diode.

The design and evaluation of 1:4 tree sensors using external address decoders are described. The designed 1:4 tree sensor using external address decoders can integrate about 16 times of pixels against using node automata. The power consumption of 1:4 tree sensors using external address decoders is estimated using `spice`, which is proportional to $O(n^{0.84})$, where n is the edge size of pixel plain, that is expected be small enough for mega-pixel image sensors.

The designs of 1:4 tree code decoders are also described, both in prototype systems using FPGAs and full-custom chip using 1.5μm CMOS technology are described, and the operation of the prototype systems is checked.

List of Presentations and Publications

Chapter 2

- J.Akita and K.Asada, "A Method of Reducing Power Consumption of CMOS Logic Based on Probability Model of Signal Transition," *Technical Report of IEICE*, ED93-83, Sep. 1993.
- J.Akita and K.Asada, "A Method for Reducing Power Consumption of CMOS Logic Based on Signal Transition Probability," *Proc. of EDAC-ETC(Europian Design Automation Conference & Europian Test Conference) Euro ASIC*, Mar. 1994.
- J.Akita and K.Asada, "A Method for Power Reduction of Finite State Circuit with Optimum State-code Assignment," *Technical Report of IEICE*, ICD94-104, Sep. 1994.
- H.Hayashi, J.Akita, and K.Asada, "A Method of Optimal State Code Assignment for Reducing Power Consumption in Synchronous Circuits," *Proc. of 1994 IEICE Fall Conference*, A-67, Sep. 1994.
- J.Akita, H.Hayashi, and K.Asada "An Estimation and Reduction of Power Consumption in Clock Line of Synchronous Flip-Flops," *Proc. of 1994 IEICE Fall Conference*, A-68, Sep. 1994.
- K.Asada and J.Akita, "Optimum State Assignment for CMOS Implementation

of Low Power Finite State Machine," *Proc. of IFIP Workshop on Logic and Arch. Synthesis*, Dec. 1994.

- J.Akita and K.Asada, "An Estimation of State Code Assignment for Low Power Finite State Circuit," *Proc. of 1995 IEICE Spring Conference*, A-108, Mar. 1995.

- K.Asada and J.Akita, "A Method for Reducing Power Consumption of CMOS Logic Based on Signal Transition Probability," *IEICE Trans. on Electronics*, Vol.E78-C, No.4, pp.436–440, Apr. 1995.

Chapter 3

- J.Akita and K.Asada, "A Signal Scanning Method of Sensors With Hierarchal Structure of Node Automata," *Technical Report of IEICE*, VLD95-62, Sep. 1995.

- J.Akita and K.Asada, "An Image Scanning Method with Data Compression using Tree Structure of Automata," *Proc. of 1996 IEICE Spring Conference*, A-43, Mar. 1996.

- J.Akita, R.Watabe, and K.Asada, "A Novel Tree Structure of Automata for Selective Scanning of Image Signals," *Proc. of the ITEC'96*, p.33, Jul. 1996.

- K.Asada and J.Akita, "Image Sensor using Tree Structure," *Symposium on Scientific Research on Priority Areas, "Ultimate Integration of Intelligence on Silicon Electronic Systems"*, Mar. 1997.

- J.Akita and K.Asada, "Image Data Compression Efficiency using Tree Scanning and Run-length Coding," *Proc. of 1997 IEICE Spring Conference*, A-6-10, Mar. 1997.

- K.Asada, J.Akita, and R.Watabe, "A Tree Structure of Automata for Selective Image Scanning and Its Implementation," *Comp. & Elec. Eng.* (to be published).

Chapter 4

- K.Asada, J.Akita, M.Nawamin, and R.Watabe, "Intelligent Lower Power Devices and Circuits," *Symposium on Scientific Research on Priority Areas, "Ultimate Integration of Intelligence on Silicon Electronic Systems"*, Mar. 1996.
- K.Asada and J.Akita, "A Selective Image Scanning Method using Tree Structure of Automata and Its Implementation," *Proc. of 1996 IEICE Fall Conference*, ES-3-7, Sep. 1996.
- K.Asada, J.Akita, and R.Watabe, "A Tree Structure of Automata for Selective Image Scanning and Its Implementation," *Proc. of 4th Int. Conf. on Soft Computing (IIZUKA'96)*, pp.113–116, Oct. 1996.

Chapter 5 and 6

- R.Watabe, J.Akita, and K.Asada. "An Implementation on CMOS Circuit of Tree Structure of Automata for Image Scanning," *Proc. of the ITEC'96*, p.35, Jul. 1996.
- J.Akita and K.Asada, "An Implementation of Image Scanning Method with Selective Activation of Tree Structure," *Proc. of 1996 IEICE Fall Conference*, A-54, Sep. 1996.
- J.Akita and K.Asada, "An Image Sensor using Quad Tree for Selective Scanning with Adaptive Resolution," *Proc. of IEEE CCD & AIS Workshop*, p.5-1, 1997.6.
- J.Akita and K.Asada, "An Image Scanning Method with Selective Activation of Tree Structure," *IEICE Trans. on Electronics*, Vol.E80-C, No.7, pp.956–961, 1997.7.
- J.Akita and K.Asada, "A CMOS Image Sensor with Variable Block Access Function," *Proc. of 1997 IEICE Fall Conference*, C-12-39, Sep. 1997.

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