Integrated Circuit 2A Examination / Integrated Circuit2 Midterm Examination

2018/11/26(Mon)　08:45～10:15@102

※ メモなし講義資料(手書きの書き込みも可)・自筆ノート・書籍のみ持込可。
※ 解答は導出過程を含めてすべて答案用紙(日本語でも英語でもよい)に記入すること。

1. Let's discuss on the architecture of adders. Assume the i-th bit of input signals A and B to be Ai and Bi, respectively, and the i-th bit of the sum and the carry output to be Si and Ci, respectively. Assume that the generation and the propagation term in i-th bit to be Gi and Qi, respectively. (40)
(1) Write Gi and Qi in Boolean expression.
(2) Write Si and Ci in Boolean expression using Gi and Qi.
(3) Write C0, C1, C2, and C3 with using the carry look-ahead architecture in Boolean expression of Ai and Bi.
(4) The propagation term, Qi, can be described using logical-OR, instead of exclusive-OR. Answer the reason why.

2. Figure 1 shows the circuit diagram or 2-input XOR gate. Show each MOS transistor's state (ON or OFF) of M1 - M6 for all four combinations of A&B, as well as output value of X. Use the circle ("○") for ON, and the cross ("×") for OFF.(20)

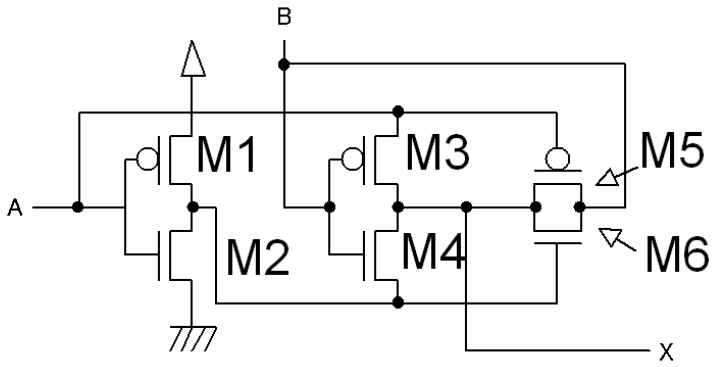

Fig.1

3. Figure 2 shows the circuit of dynamic AND gate. Show the timing diagram of the output X for the input of A, B, and ϕ in Fig.3. Describe X as well as A, B, and ϕ.(30)

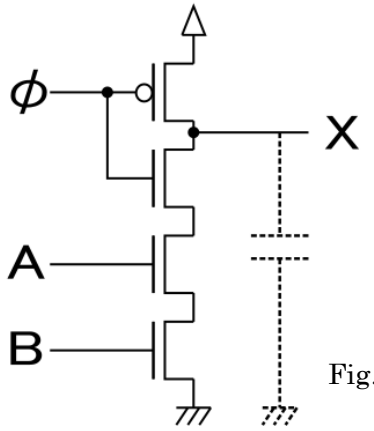

Fig.2

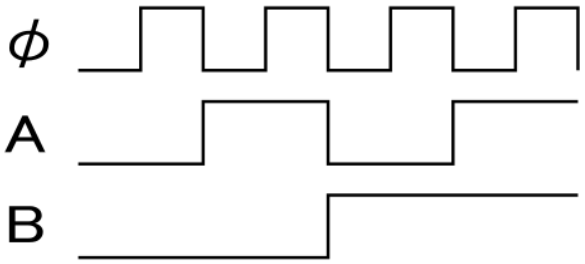

Fig.3

4.【予告問題】Discuss the topic on "MOSFET's Scaling, or Moore's Law" in terms of social, technical, and economical impacts. Your opinion AND your personal experience MUST be included. Write it down on A4-size paper (hand-written material only, in Japanese or English). (10)