Integrated Circuit 2B: Examination

※ メモなし講義資料(手書きの書き込みも可)・自筆ノート・書籍のみ持込可。

※ 解答は導出過程を含めてすべて答案用紙(日本語でも英語でもよい)に記入すること。

1. Figure 1 illustrates the circuit diagram of SRAM cell array of 2x2 bits, where each cells has the initial state as illustrated. Answer the waveform of DL0, DLb0, DL1, and DLb1 in case of the control signals in Fig.2 are given. Note that equalization circuit, activated by EQ, is adequately configured. The timing of signal transition must be clearly indicated by vertical dotted line.(40)
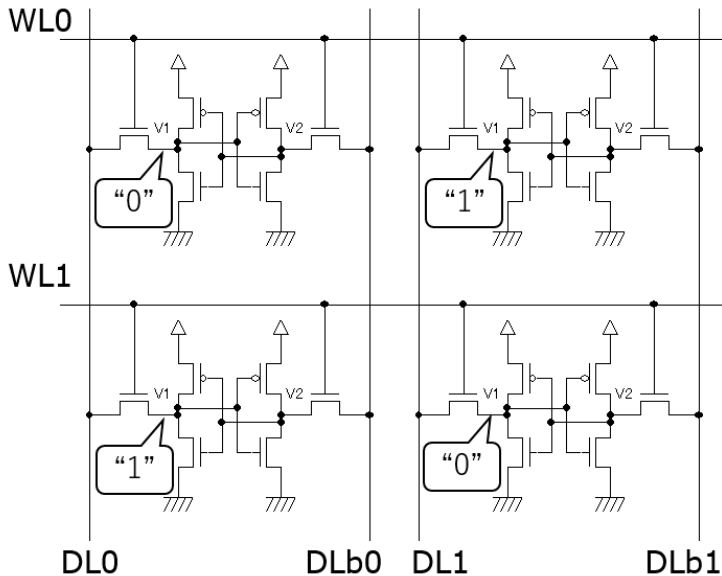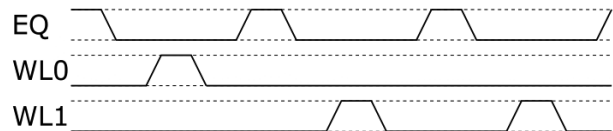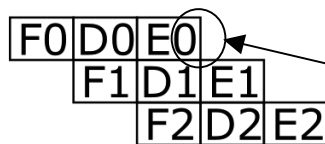

Fig.1

Fig.2

2. Let's consider the RISC microprocessor that executes all the instructions with three stages of F (fetch), D (decode), and E (execute). Answer the pipeline operation as an example when executing the program in Fig.3, with address of execution. Note that "mov" indicates the move operation, and "jmp" indicates the jump operation to the specified address. (30)

Fig.3

3. Left of Fi. 4 shows the circuit diagram of cascade amplifier. Answer its small signal equivalent circuit (小信号等価回路). Assume that the adequate bias voltage is applied, and use the small signal equivalent circuit of MOS transistor in Fig.4. Note that all the variables must be defined. (20)

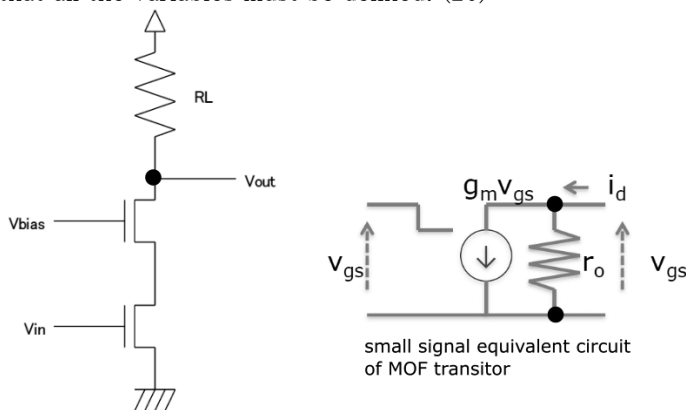small signal equivalent circuit of MOF transitor

Fig.4

4. Describe your reflection (振り返り) and impressions on what you have learnt in this class, in terms of how they effect your daily and long term life, and the context you have learnt in other classes. (10)