Integrated Circuit C Examination

2020/11/30(Mon)　08:45～10:15@108

※ メモなし講義資料(手書きの書き込みも可)・自筆ノート・書籍のみ持込可。
※ 解答は導出過程を含めてすべて答案用紙(日本語でも英語でもよい)に記入すること。

1. Figure 1 shows the circuit diagram of 3bit Manchester Carry Chain. Note that Q_n and G_n are the propagation and the generation term derived from A_n and B_n, and $\overline{PR}$ is pre-charge control signal. (50)
(1) Describe Boolean expression of Q_n and G_n using A_n and B_n.
(2) Describe Boolean expression of C_0, C_1, and C_2 using A_0 - A_2 and B_0 - B_2.
(3) Show all the possible discharge paths of X after pre-charge for cases of (a)A=001/B=001, (b)A=011/B=001, (c)A=101/B=001, and (d)A=111/B=111. Indicate discharge path as a series of the MOSFET's name along the path. For example, for the dotted path in Fig.1 is described as "M8-M6-M7". Note that "A=001" means A_2= A_1=0 and A_0=1

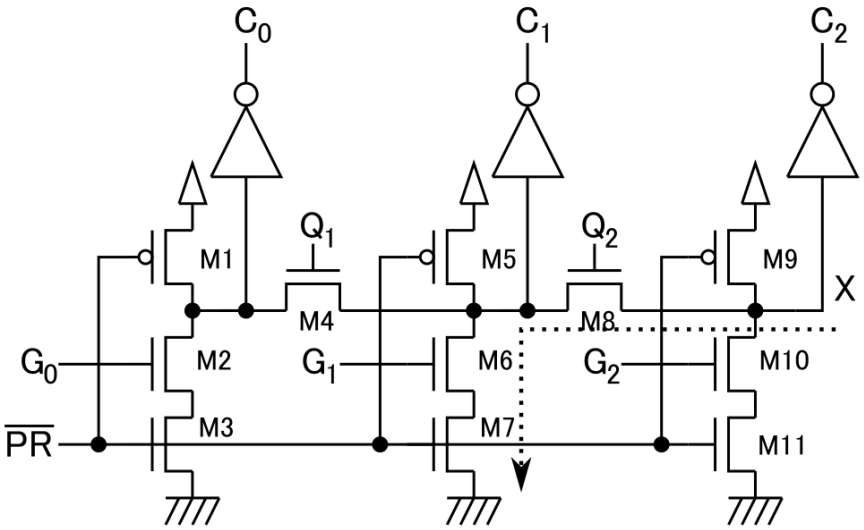

Fig.1

2. The total execution time of a program, T, is defined as N×CPI×T, where N, CPI, and T are the number of instructions to be executed in a program, the number of clock cycle per instruction, and the clock cycle time, respectively. Assume that processors A and B has the specifications as shown in Tab.1. Here, "Average N" means the average of number of instructions to be executed in a program.(25)

Processor	A	B
Instruction Set Type	CISC	RISC
Average N	10	50
CPI	4	1
Controller Area [mm^2]	5.0	1.0

Tab.1

(1) Calculate the minimum clock frequency of the processor B that achieves the higher performance than the processor A operating at 100[MHz].
(2) Calculate the possible cache size in [MB] for the processors of A and B for the total chip area of 6.0[mm^2]. Here, the cache area of 1[MB] is 1[mm^2].
(3) By using the advanced (scale-downed) technology, the area of the controller and cache are scaled in 1/2. Calculate the possible cache size in [MB] for the processors of A and B for the total chip area of 6.0[mm^2],

3. Discuss the pros and the cons of the ripple carry adder compared with the carry look-ahead adder (CLA). The following keywords MUST be included: carry propagation delay(キャリー伝搬遅延), circuit complexity(回路の複雑さ), circuit regularity(回路の規則性)(15)

4.【予告問題】Discuss the topic on "MOSFET's Scaling, or Moore's Law" in terms of social, technical, and economical impacts. Your opinion AND your personal experience MUST be included. Write it down on A4-size paper (hand-written material only, in Japanese or English). (10)